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RESEARCH ARTICLES

Exploitation of the nonlinearities in electromagnetic energy harvesting and passive UHF RFID

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In this paper, some theoretical aspects and experimental results are discussed with the aim to provide supplementary dc energy to radio frequency identification (RFID) tags by exploiting the nonlinear nature of rectifier devices. Three nonlinear phenomena are treated: (i) the impedance power dependence, (ii) the harmonic production, and (iii) the dependence on the radio frequency waveform. The novelty of the work relies on proposing a double rectifier composite system in where the nonlinearity of each rectifier is exploited to enhance the global powering performance of the system. Using the passive RFID technology as a beacon for the implementation, the approach considers combining the internal rectifier circuit of a commercial RFID chip operating at 868 MHz with an external rectifier circuit operating at 2.17 GHz. The solution triggers in a composite system RFID tag-harvester integrated in a single-feed dual-band antenna. The experimental validation shows 5 dB of tag sensitivity enhancement when it is empowered by the external harvester. The enhanced sensitivity produces an increase in the theoretical reading range distance from 3.3 to 6.1 m.

Keywords: Antennas and propagation for wireless systems, Harmonic balance, Harvesting, Microwave measurements, Modeling and measurement, Passive RFID, RFID and sensors, Wireless power transfer

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I. INTRODUCTION

The development of the internet of things, smart cities or smart houses is expected to rely on Wireless Sensor Networks (WSN) composed of a huge number of interconnected electronic devices. Powering networks through cables or batteries may become almost impossible but mostly unpractical not to mention the adverse environmental effects [1]. According to Koomey estimations, the total energy needed for a computational operation decreases by 50% each 18 months [2]. An example of this less powering evolution is the low-consumption passive radio frequency identification (RFID) tags: in 1997, the tag sensitivity was of −8 dBm, while nowadays it is only about −22 dBm [3]. Consequently in a near future, the harvesting solutions could completely satisfy the power needs of devices for the WSN. In this context, the use of passive tags could be very relevant because of their capabilities to integrate sensor functionalities while always benefiting from their advantages, i.e. wireless and battery-free [4–8]. With this motivation, new techniques of energy harvesting and methods to enhance the performances are a worldwide hot research topic [9–14]. These techniques have been addressed in the literature in a direct or indirect manner by considering the nonlinear behavior of electromagnetic energy harvesting (EEH) devices. Actually, it is possible to classify the treatment of these nonlinear behaviors in three main categories: (i) impedance-power dependence [15–17], (ii) harmonic generation [18–20], and (iii) waveform design [21–24].

This paper proposes an approach to exploit these nonlinear phenomena using the passive RFID technology as the beacon for the implementation. The objective is to provide additional energy to the chip, allowing it to increase its sensitivity and consequently its read range. The proposed design combines the internal rectifier circuit of a commercial RFID chip operating at 868 MHz with an external rectifier circuit operating at 2.17 GHz both connected to a common single-feed dual-band antenna. The nonlinearity of each device is exploited in order to improve the global performance of the system, hereinafter the so-called RFID tag-rectenna (RFID-TR).

This paper is organized as follows. Section II presents the composition and operation of the RFID-TR system and the proposed method in order to enhance the conversion efficiency of rectifying devices. Section III details the optimized design of the composite system highlighting the exploitation of the nonlinear behavior of rectifiers. Section IV shows the evaluation results of the realized prototype and discusses the scope of the approach. Finally, Section V draws final conclusions and perspectives.

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II RFID-TR SYSTEM

A) Architecture

The system architecture of the RFID-TR based on a double rectifier configuration is depicted in Fig. 1. The RFID-TR is mainly composed by: (i) the RFID section (including the so-called first rectifier) operating at 868 MHz, (ii) the EEH section (including the so-called second rectifier) operating mainly at 2.17 GHz, and (iii) a common dual-band antenna that serves as radiating element in order to communicate with the two external radio frequency (RF) sources.

The RFID section is in charge of the classic RFID link, including data information and energy harvesting. A distributed network integrated to the antenna matches the RFID chip impedance at 868 MHz. An EM4325 RFID chip (TSSOP-8 package) is used, because it offers a supplementary dc input pin in order to operate in battery-assisted power (BAP) mode [25, 26]. The supplementary dc power allows the chip to enhance its activation sensitivity. The BAP mode will be later used in order to validate the proposed approach.

The EEH section is in charge of the generation of complementary power harvesting it from a 2.17 GHz signal combined with the third-harmonic generated by the chip [20] looking for an enhancement in the RF-to-dc conversion efficiency. A lumped matching network ensures the power transfer from the antenna, which has the RFID section connected, toward the rectifier diode at 2.17 GHz. An external RF source intended to belong to the Universal Mobile Telecommunications System (UMTS) band generates the 2.17 GHz signal. As proof of concept, it is worth noting that the 2.17 GHz signal does not consider any modulation. The rectifier element is an HSMS 2860 Schottky diode (SOT23 package) [27]. The integration of the double rectifier system allows it to inject the harvested energy by the EEH section into the RFID section enabling to increase the chip sensitivity and so to enhance the RFID-TR read range.

Finally, the double rectifier configuration, which intrinsically considers a double source operation (at 868 MHz and 2.17 GHz) as shown in Fig. 1, favors the powering performance of the RFID-TR because the design approach considers the nonlinear effects of each rectifier in a simultaneous operation. In other words, the described architecture aims to optimize the RFID-TR operation in terms of power generation in the EEH section and RFID communication exploiting the three nonlinear phenomena of diode-based circuits previously evoked and further detailed in the next paragraph.

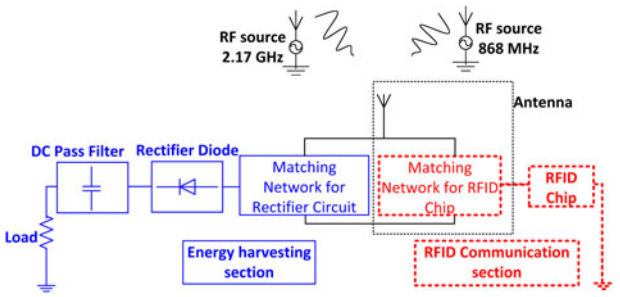

Fig. 1. Architecture of the RFID-TR system. The system consists of an EEH section (solid line), an RFID section (dash line), and a single-feed antenna.

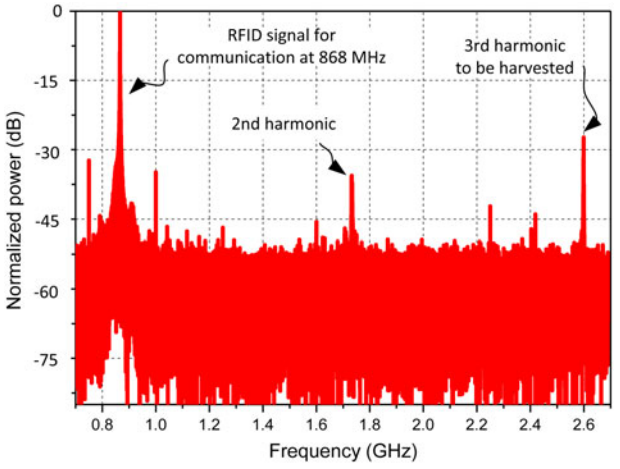

Fig. 2. Normalized power spectral density of the tag response measured at the activation threshold of the chip under test [25].

B) Treating the nonlinearity of EEH devices for conversion enhancement

1) IMPEDANCE-POWER DEPENDENCY

Due to the variable resistor and capacitor feature of rectifying diodes, the impedance of diode-based rectifier circuits is nonlinear dependent on the voltage [28]. This property led to consider a specific input power from which the design is optimized [15–17]. For the RFID-TR, the design should ensure: (i) the power transfer from the RFID reader toward the RFID chip at 868 MHz; (ii) the power transfer from the RFID chip toward the EEH section at the third harmonic (i.e. 2.604 GHz) in order to harvest this wasted power [29]; and (iii) the power transfer from the 2.17 GHz source toward the EEH section. To achieve this operation, the matching networks of the RFID-TR system have to be optimized taking into account certain priorities: both RFID section and EEH section have to operate at −10 dBm at 868 MHz and 2.17 GHz, respectively. This value prioritizes the RFID chip activation [25].

2) HARMONIC GENERATION

The nonlinear i–v characteristic of a diode imposes a current signal to be composed by fundamental and harmonic components in function of the voltage operation. Most energy-harvesting circuits already contain a bandpass filter on the antenna input that permits the fundamental frequency to enter, but reflects the harmonics back into the energy harvester. This technique, very common in the high-efficiency energy harvester design, allows maximizing the conversion efficiency by confining all the higher order harmonics between the low-pass filter and the dc pass filter [30]. Furthermore, harmonic treatment techniques such as the Class-E or Class-F rectifier [28] help to confine the energy carried by harmonics in order to optimize the conversion efficiency of rectifier circuits. The presented impedances to the rectifier circuit (at fundamental and harmonic frequencies) enable that the stored energy in the diode is not self-dissipated, but rather released to the load.

The harmonic treatment can be addressed in a design stage by simulation tools such as the harmonic balance [19, 20]. Figure 2 shows the normalized power spectral density (PSD)

of the EM4325 RFID chip response measured using a similar method to the one reported in [20]. The setup considers the chip activation threshold power, the reader harmonics suppression, and the chip impedance matching at fundamental frequency as in common tags. At the chip activation threshold, the level of harmonic signals is significant at 1.736 GHz (second harmonic) and at 2.604 GHz (third harmonic), considering the scope of backscattering applications.

Therefore, this paper proposes to exploit the chip harmonic generation in order to create a composite signal at the second rectifier input [29]. This composite signal is composed by the third harmonic product of the RFID chip and the 2.17 GHz carrier wave (CW). The impact of the signal composition on the RF-to-dc conversion efficiency of the EEH section is studied in the next section.

3) WAVEFORM DEPENDENCY

When a rectifier circuit is excited simultaneously by more than one signal relative to a single carrier of the same average power, its nonlinear i–v characteristic can potentially lead to an enhanced RF-to-dc conversion efficiency. Indeed, a composite signal of a number of tones (i.e. a multi-harmonic) represents a signal with a time-varying envelope (i.e. the presence of instantaneous power peaks) and a certain peak-to-average-power-ratio (PAPR). The greater the PAPR is in the input signal, the greater is the RF-to-dc conversion efficiency of the rectifier. Furthermore, a time-varying envelope signal is capable to activate the rectifying devices for lower average input power levels compared with signals of constant envelope and the same average power. However at high-power levels, the PAPR decreases the conversion efficiency [21–24, 31].

Thereby, the combination of the CW at 2.17 GHz (i.e. a constant time envelope signal), and the ASK modulated third-harmonic product of the RFID chip produces a time-varying signal with higher PAPR than the one of a single CW signal. In the RFID-TR, the waveform dependency is then exploited by feeding the EEH section with a composite signal, i.e. a time-varying envelope signal that is used to boost the RF-to-dc conversion efficiency.

4) SUMMARY AND DESIGN REQUIREMENTS

The role of the RFID section is to ensure the RFID communication, and at the same time, to produce a third harmonic that will be exploited in the EEH section in order to improve the RF-to-dc conversion efficiency.

Actually, the harmonic reflection from the RFID chip toward the EEH section performs two tasks that drive the RFID-TR design: (i) to prevent losing the energy which is converted into harmonics that could impairs the efficiency of the RFID section; (ii) to redirect efficiently the harmonic power toward the EEH section. It is worth noting that the harvesting performance of the RFID section is not studied in the design because of the use of a commercial RFID chip. Therefore once the chip activation condition considering optimum impedance matching at 868 MHz is achieved, the design technique focuses on the harmonic production of the chip. To maximize the dc output of the EEH section, an electric and electromagnetic co-simulation method will optimize the impedance matching networks composed by lumped and distributed elements. Such an optimization is obtained by analyzing the spectral components at the inputs of both sections and the output of the EEH section.

One notices that the design method indirectly performs a similar task to the one performed by Class-E or Class-F rectifiers in [15, 28], where the matching networks or line terminations present impedances at the fundamental and harmonics components in order to force the diodes to operate efficiently (i.e. dissipating in its non-conducting cycle, all the stored energy during its conducting cycle).

III. DESIGN PROCEDURE

From the presented architecture, and exploiting the harvesting enhancement techniques explained in Section II, the design procedure of the RFID-TR prototype is sequentially described below.

1. The impedances of the RFID chip and the rectifier diode, with respect to the incident RF power and frequency, are measured before the antenna design (Section A).
2. An equivalent nonlinear model of the RFID chip and the rectifier diode is built in an electrical simulator, taking into account the impedance characterization (Section B).
3. The common antenna is designed considering complex impedance matching techniques (Section C).
4. An electrical and electromagnetic co-simulation integrates each electrical model and the antenna for a global optimization of the RFID-TR (Section D).

Note that the design process is valid for all kind of passive RFID chips, rectifier diodes, and antenna structures, regardless the frequency or power chosen.

The CST suite is used for the simulations: Design Studio for the electrical simulations and Microwave Studio for the electromagnetic ones, and the combination of these tools for the co-simulation procedure.

A) Impedance measurement of nonlinear devices

Using a test platform similar to the one presented in [20], the passive RFID chip and the rectifier diode are measured separately at the frequencies of interest: at 868 MHz (RFID fundamental frequency), 2.17 GHz (UMTS band) and 2.604 GHz (RFID third harmonic). The measurement method consists of three parts:

- Fixture of the device under test (DUT);
- Calibration of the fixture (de-embedding) and complete calibration of the network analyzer at the measurement reference plane and at a fixed exploitation power;
- Measuring of the DUT.

The network analyzer is configured with an external source in order to generate an RFID query signal and so to activate the RFID chip during the measurement procedure. Specific details about the method can be found in [20].

Figure 3 shows the measured impedance for both the RFID chip at 868 MHz and for the Schottky diode at 2.604 GHz, in function of a power sweep from −20 to 0 dBm. The RFID chip impedance is more sensitive to power changes than the diode impedance. For the proof of concept, given the nonlinear variations of the impedance in function of the input power, the impedance values for the step 2 are considered at −10 dBm input power in order to prioritize the activation

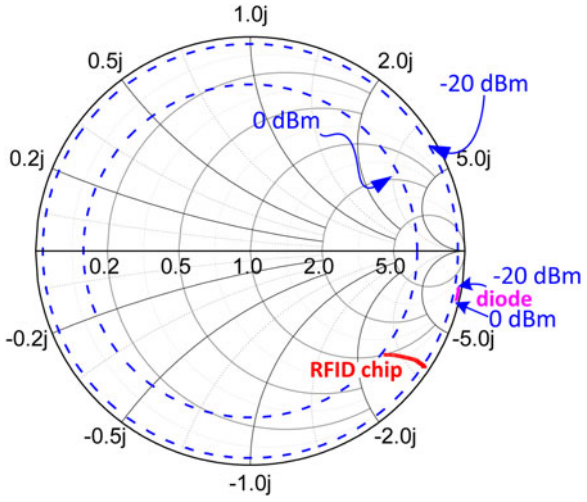

Fig. 3. Measured impedance in function of a power sweep from −20 to 0 dBm for: (a) the RFID chip at 868 MHz and (b) the rectifier diode at 2.604 GHz.

Table 1 Measured impedances of RFID chip and diode at −10 dBm input power.

Device	Impedance at 868 MHz (Ω)	Impedance at 2.17 GHz (Ω)	Impedance at 2.604 GHz (Ω)
RFID chip	$18 - j130$	–	$6 - j49$
Diode	–	$72 - j242$	$51 - j211$

power of the chip and ensure the RFID communication. This first assumption allows proposing equivalent circuits that could be optimized by simulation in order to ensure the cohabitation of the two rectifiers operating each one at a given input power. Furthermore for the RFID chip, this value of input power is kept constant during the optimization procedure. All measured impedances for both RFID chip and rectifier diode at −10 dBm input power are summarized in Table 1 (note that the chip impedance given in the datasheet at 868 MHz is $23 - j145\ \Omega$).

Because MOSFET transistors are integrable in CMOS fabrication process, it is worth noting that rectifier circuits could be designed in CMOS technology, using MOSFET transistors connected in diode configuration However, given the modular integration followed in the proposed study (antenna, RFID chip, diodes, etc.) the use of rectifier circuits in CMOS is out of the scope of the paper.

B) Electrical modeling of nonlinear devices

1) RECTIFYING DIODE MODEL

The architecture of the EEH section is shown in Fig. 4. It consists of a single Schottky diode which rectifies the RF input and a capacitor that continuously charges and discharges producing at its output a dc signal feeding a load resistor. The capacitor also filters the RF components that may impairs the dc output and degrades the conversion efficiency of the diode. In order to consider the nonlinear behavior of the diode, its Spice model is used. The HSMS 2860 diode presents the following electrical parameters: low series resistance $R_s = 6\ \Omega$; zero-bias junction capacitance $C_{jo} = 0.18$ pF;

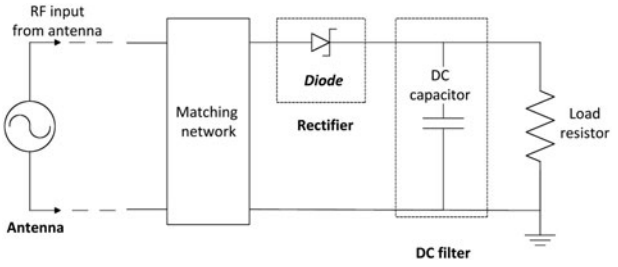

Fig. 4. EHH section of the RFID-TR.

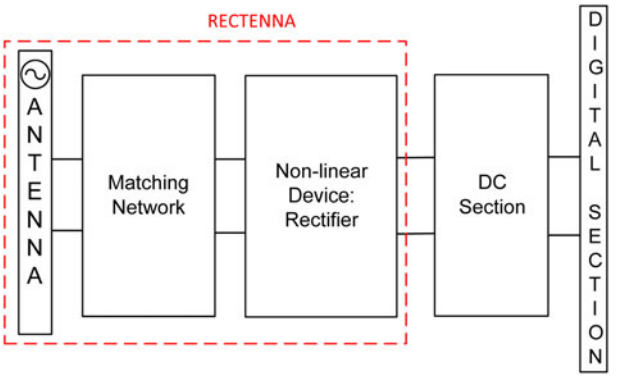

Fig. 5. Functional architecture of a passive RFID tag.

breakdown voltage threshold $V_{br} = 7$ V; detection sensitivity of 35 mV/uW [27]. The proposed electrical model does not consider the package parasitic effects, but ensures a rectifier circuit with similar conversion efficiency than a real sample including nonlinear features (i.e. impedance-power dependency and harmonics generation [32]).

2) RFID CHIP MODEL

An RFID tag architecture is shown in Fig. 5 highlighting the rectenna section. It consists of an antenna, a matching network and a rectifier circuit based on a Dickson topology with two or more diode-based voltage doubler stages [33]. The rectifier circuit, responsible of the nonlinear behavior of the RFID chip, determines the RFID chip sensitivity, the capacitive nature of the RFID chip impedance and the harmonic production with specific predominance of odd or even harmonics depending on the chosen rectifying architecture [33].

From the measured impedances (Fig. 3) it can be concluded that the chip is the most critical parameter regarding the impedance-power dependency, hence the importance of prioritizing the measured values at −10 dBm as reference to build the RFID chip model. Therefore a diode-based RFID chip model is simulated with the aim to produce a similar impedance and harmonic generation to the one characterized at −10 dBm. The variable parameters are the number of diode-based voltage multiplier, the capacitors values, and the resistor at the input.

The proposed equivalent circuit results in a three-stage voltage multiplier using HSMS 2860 Schottky diodes, with coupling capacitors (*Cc*) and ended in a dc load resistance (*Load*) as shown in Fig. 6. Additionally, a tuneable shunt resistor (*Rin*) and a tuneable shunt capacitance (*Cin*) are set at the input in order to tune small impedance variations due to the package. The design parameters for the RFID chip model are:

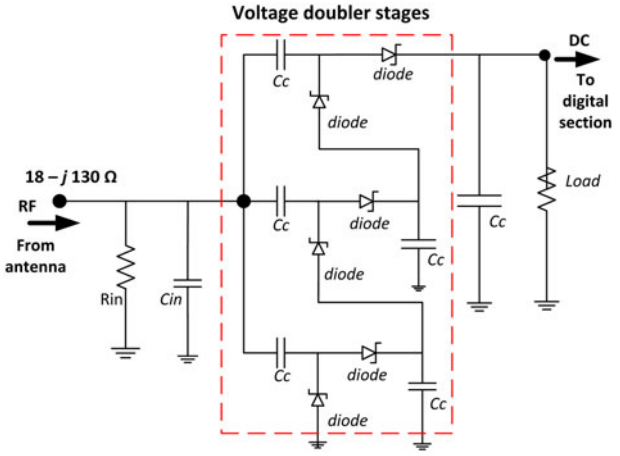

Fig. 6. RFID chip equivalent circuit with three voltage-doubler stages based on Dickson topology.

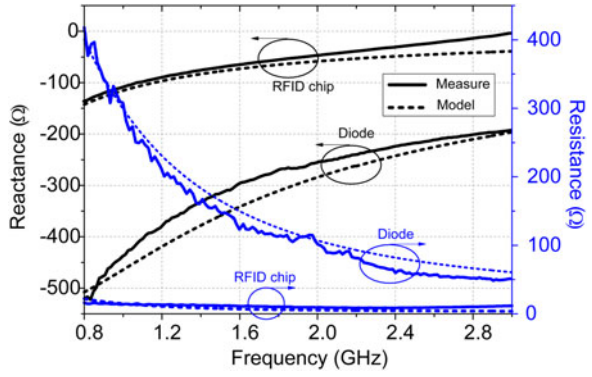

Fig. 7. Measured and modeled impedances for the RFID chip and the Schottky diode at −10 dBm.

$Cc = 4.3$ nF; $Cin = 0.146$ pF; $Rin = 965\ \Omega$; $Load = 10$ kΩ. The circuit model takes into account the harmonic generation and presents an input impedance close to the one measured for the RFID chip ($18 - j130\ \Omega$).

Finally, Fig. 7 compares the measured and modeled impedances for the RFID chip and Schottky diode for an input power at −10 dBm. As expected, the best fitting for the RFID chip is observed around 868 MHz. The proposed models are also found valid for the other frequencies points (notably at 2.17 and 2.604 GHz). With these nonlinear models, a common antenna is designed in the next section.

Under the assumption of having an optimal commercial RFID chip which activates at −10 dBm, the proposed equivalent model is not evaluated in terms of its RF-to-dc conversion efficiency, but in terms of its impedance and harmonic production supported by experimental measurement. To consider the harvesting performance of the model, some changes may be considered in the architecture by reducing to the minimum the losses (e.g. removing the input resistor) and properly tuning the capacitor values.

C) Single feed dual-band antenna design

Considering the dual-band operation requirements, the chosen antenna topology is inspired from [34] where a modified L–F inverted antenna is presented. The antenna structure

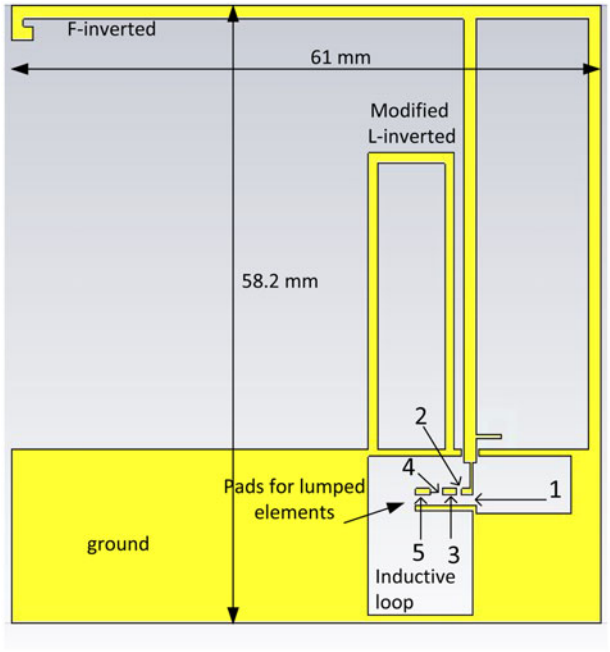

Fig. 8. Structure of the single-feed dual-band antenna. The arrows indicate the pads (i.e. ports) where the lumped elements of the EEH section are connected. The pads are considered in the electromagnetic simulation.

allows the use of a ground plane for the rectifier circuitry and a radiator for the RFID communication and rectenna functions, all in a common one side. Using RFID antenna design techniques such as inductive loops to cancel the capacitive impedance of RFID chips and meandering size reduction [35, 36], the single-feed dual-band antenna is designed and shown in Fig. 8. Two loops in the ground plane allow the inductive impedance matching to compensate the capacitive effect of devices connected at the antenna input (i.e. the RFID chip and the EEH circuit). Rogers RO4003 substrate with 3.55 permittivity, 0.003 loss tangent and 0.8 mm thickness is used for the prototype. The electromagnetic simulation is performed from *DC* to 10 GHz in order to cover the first fifth harmonics of the 868 MHz for the RFID section and the fourth harmonics of 2.17 GHz for the EEH section. Pads in where lumped components are soldered are also considered in the electromagnetic simulation. The antenna design procedure is driven by optimization processes (using CST). The optimization goals are: minimum reflection coefficient and maximum gain at both 868 MHz and 2.17 GHz frequencies. The initial design considers the capacitive impedance of the RFID chip as antenna load all along the frequencies of interests in order to mainly define the resonant elements (modified "L" inverted and modified "F" inverted) and the inductive matching (with the loops in the ground).

D) Co-simulation design of the RFID-TR system

The integration of the nonlinear circuits and the antenna is simulated in an electric-electromagnetic cooperation environment. The aim of the co-simulation is to optimize the antenna structure and the lumped element values, taking into consideration the nonlinear behavior of RFID and EHH sections. A co-simulation project is defined: (i) for the electromagnetic

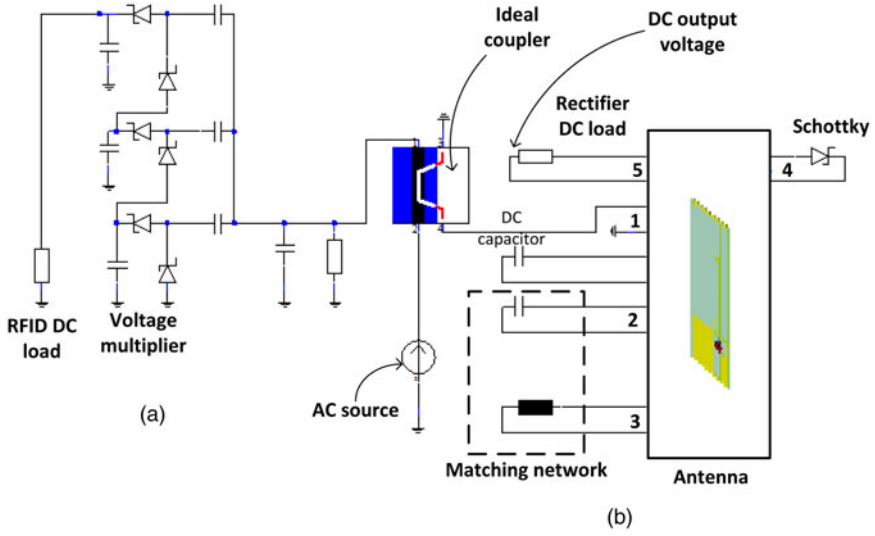

Fig. 9. Electric-electromagnetic co-simulation of the proposed RFID-TR: (a) nonlinear model of the RFID chip and (b) co-simulation integration of the RFID-TR.

part the Time Domain Solver is used in Microwave Studio, and (2) for the circuit part "*S*-parameters" and "Spectral Lines" tasks from Design Studio are used. The co-simulation methodology is performed by two stages.

- The first stage aims to build the impedance matching networks considering the measured *S*-parameters of the diode and RFID chip and combining the electric and electromagnetic simulation tools. The simulation considers as optimization variables both the antenna structure (mainly the dimensions of inductive loops) and the lumped components values (complementary lumped matching network at 2.17 GHz). The optimization goals are to minimize the reflection coefficient at 868 MHz and 2.17 GHz at the antenna input considering the components connected. At this stage, the simulation does not consider the nonlinear models.
- The second optimization stage considers the lumped components as variables, and takes into account the equivalent nonlinear models of diode and RFID chip [37]. The optimization goal is to maximize the dc output of the EEH section. An input power of −10 dBm into the RFID chip and the rectifier diode is always considered at 868 MHz and at 2.17 GHz, respectively. It is worth noting that the impedance modulation of the RFID chip produces small variations of the impedance seen by the antenna at the upper frequencies. However, it was experimentally demonstrated that the modulation index performed by the chip decreases as the frequency increases [20]. Therefore, although the small variations are not considered in the simulation procedure, the impedance modulation will not produce considerable mismatching with the antenna matched to only one impedance state.

Regarding the dc section, a 3 kΩ load resistance represents the measured impedance of the BAP pin of the chip. Figure 9 presents the block diagram of the second co-simulation stage integrating all the sections of the proposed RFID-TR system. An ideal directional coupler is used to integrate the *S*-parameters of the antenna with the RFID chip model and an AC source. The co-simulation provides an optimized lumped impedance matching network at 2.17 GHz composed by a 0.2 pF series capacitor and a 6.8 nH shunt inductor.

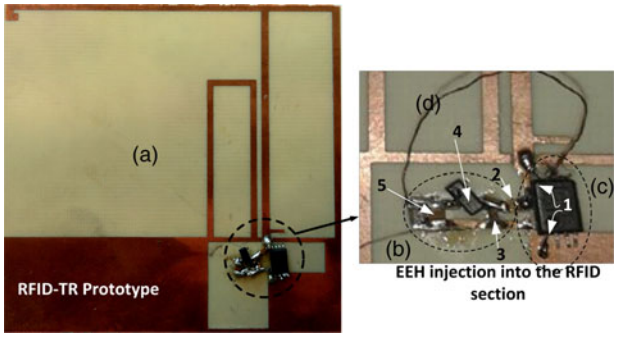

Fig. 10. Prototype of the RFID-TR: (a) dual-band antenna, (b) EEH section, (c) EM4325 RFID chip, and (d) connection for harvested dc power. The arrows' numbers indicate the ports where the lumped elements are soldered.

The main difference of the proposed co-simulation method with respect to Class-E or Class-F rectifier methods is that the impedance presented at the rectifier is not independently controlled at each frequency but globally controlled by the two optimized matching networks (the distributed network at 868 MHz and the lumped one at 2.17 GHz) thanks to the spectral analysis at the section input (i.e. by maximizing the power transfer at the different RF frequencies) and EEH output (i.e. by minimizing the PSD of RF frequencies and maximizing the dc component). The final goal is to maximize the conversion efficiency of the EEH section. This operation allows the EEH section to cohabit and profit from the RFID section considering that the operation power levels may be different for each section. It is also worth noting that the multi-device waveform effect is not simulated but experimentally proven, therefore the benefit of the effect is not estimated in *a priori* analysis

1) PROTOTYPING

Finally the realized RFID-TR is shown in Fig. 10. The RFID chip and lumped components are soldered at the pads. A wire is used to inject the harvested dc power into the BAP

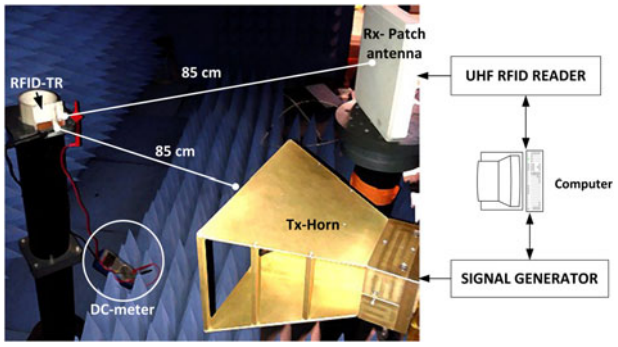

Fig. 11. Measurement setup for the performance evaluation of the RFID-TR.

input of the chip. One notices that the prototyping method (i.e. soldering and components orientation) could impair the performance of the devices and produce deviation from expected results. Actually the extra wire connected into the BAP pin of the RFID chip could add some inductance and impairs the expected operation.

The performance of the RFID-TR will be evaluated at the frequencies of interest (868 MHz and 2.604 GHz) and under the standard RFID power regulations in Europe, i.e. 35.15 dBm effective isotropic radiated power (EIRP).

IV EXPERIMENTAL RESULTS

A) Measurement setup

To evaluate the performance of the RFID-TR, the measurement procedure has two goals: (i) to measure the dc output across the load resistor in the EEH section (Section IV.B), and (ii) to evaluate the RFID tag performance of the RFID-TR in terms of read range (Section IV.C). The measurement setup shown in Fig. 11 is performed in the anechoic chamber and it is composed by:

- an Agilent N5182A signal generator, which produces a CW at 2.17 GHz, associated with a 7 dB gain horn antenna used for the transmission;
- an Impinj Speedway *R*420 Revolution RFID reader operating at 868 MHz, associated with a circularly polarized 6 dB gain antenna is used;
- a dc voltmeter connected at the load resistor in order to measure the harvested dc voltage;
- a computer in order to control the equipment for data acquisition and processing.

The setup calibration considers the antenna gains, free space propagation losses, and cable losses. Given the multi-source operation (with the RFID reader at 868 MHz and the signal generator at 2.17 GHz), three different transmission configurations are considered in order to better evaluate the operation of the RFID-TR. Table 2 presents the three considered cases.

B) EEH evaluation

Experiments when the RFID reader transmits the maximum allowed power 30 dBm, and the external source is turned-off, i.e. in the case (*a*), a weak 5 mV dc is measured at the BAP pin. Actually even if the EEH section is optimized at 2.17 GHz, the second and third harmonics of 868 MHz are being rectified in

Table 2 Transmission configurations for the RFID-TR evaluation.

Case	Transmission configuration
(*a*)	Power sweep of RFID reader signal generator turned-off
(*b*)	Power sweep of signal generator RFID reader turned-off
(*c*)	Power sweep of signal generator RFID reader fixed at 30 dBm

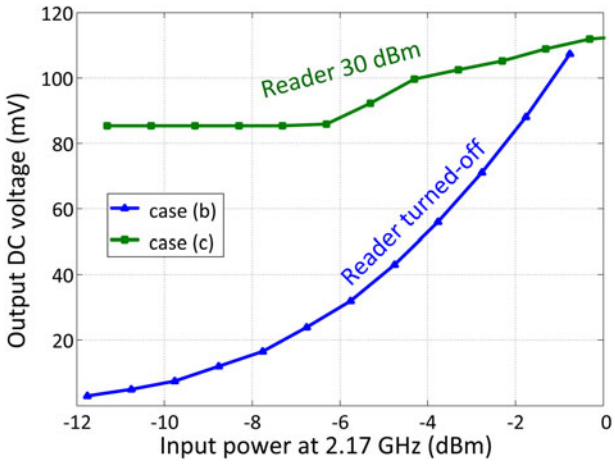

Fig. 12. Rectified dc output voltage in function of the input power at 2.17 GHz for cases (*b*) and (*c*) presented in Table 2.

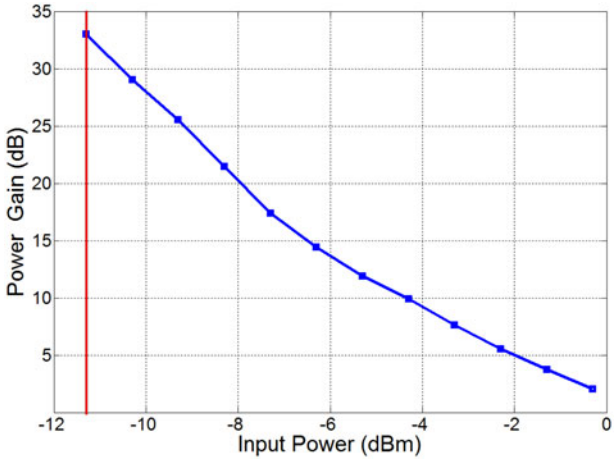

Fig. 13. Power gain as function of input power.

case (*a*). Figure 12 shows the rectified dc voltage measured at the BAP pin in function of the received input power at 2.17 GHz for cases (*b*) and (*c*), calculated using Friis formula under the setup shown in Fig. 11. When the reader is turned-off (case (*b*)), the dc voltage rises with the input power at 2.17 GHz. Finally the case (*c*) clearly shows the mutual benefit due to a joint operation of RFID chip and a rectifying circuit.

To quantify the effect of the multi-source operation, a power gain figure (G_P) is defined in (1) [21]. The factor G_P defines the power gain obtained in case (*c*) regarding to the power gain obtained in case (*b*). Since the dc load resistance

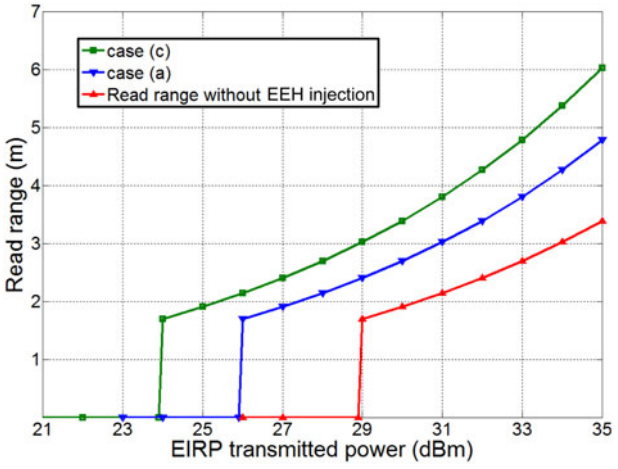

Fig. 14. Read range for the RFID-TR.

Table 3. Maximum read range without and with EEH injection.

Case	Without EEH injection (m)	With EEH injection (m)
(*a*)	3.3	4.8
(*c*)	3.3	6.1

is in both cases the same, the dc power can be defined as function of the dc voltages V_b and V_c, for the cases (*b*) and (*c*) respectively. It is worth noting that, contrary to [21] in where a similar input power is considered in the comparison, the factor G_P defined in this paper includes the gain due to the additional input power supplied by the RFID reader in case (*c*).

$$G_P = 10\log_{10}\left(\frac{V_c^2}{V_b^2}\right). \quad (1)$$

Figure 13 shows the calculated G_P. A greater cooperation effect can be observed at low-input power, i.e. between −11.3 and −7 dBm. The results are in agreement with the design stage in what concern the optimized operation about −10 dBm. A G_P 33 dB higher is obtained when the RFID-TR operates under multi-source configuration compared with the case operating only with the signal generator.

C) Read range evaluation

The RFID tag performance of the RFID-TR is evaluated by calculating its read range [38] using a Speedway Revolution RFID reader [39] for the two cases (*a*) and (*c*). Figure 14 shows the read range variations with respect to the Reader Equivalent Isotropically Radiated Power (R_{EIRP}) and compares the results with the scenario without EEH injection. Table 3 summarizes the read range results at 868 MHz.

The EEH injection in case (*c*) allows one to read the RFID-TR at lower R_{EIRP} (i.e. 24 dBm and approximately 2 m read range). Furthermore, when the RFID-TR without EEH injection is read at 35 dBm R_{EIRP} for instance, its maximum read range is 3.3 m, while with EEH injection the read range is 1.5 m higher for case (*a*) and 2.8 m higher for case (*c*). The read range enhancement is produced by a different behavior in each case. In case (*a*), even if the EEH section is tuned at 2.17 GHz, the modulated harmonics produced by the RFID chip are harvested producing the 1.5 m read range enhancement. In case (*c*), the improvement is due to the harvesting operation at 2.17 GHz but also because there of the combined effect of both RF sources producing a signal with higher PAPR.

V. CONCLUSION

This paper proposes an original design of an RFID tag that embeds an additional rectifier circuit in order to efficiently produce complementary dc power benefiting from multi-source operation and nonlinear effects in the RFID chip. The proposed solution, so-called RFID-TR, is realized and tested via a prototype that integrates an RFID chip operating at 868 MHz, an EEH circuit operating at 2.17 GHz and a common single-feed antenna. The design methodology describes each design step and the procedure to integrate the RFID chip with the external EEH circuit using the common dual band antenna. The experimental results show the enhancement of the harvesting efficiency of the EEH circuit, and also the possible enhancement of the read range when the dc power is injected in the tag itself. The beneficial effect introduced by the double rectifier and multi-source operation is based on the exploitation of the nonlinearities of each rectifier. The proposed design exploits the harmonic generation of the RFID chip and considers the impedance-power dependency of each rectifier in the integration procedure. Additionally, a time-varying envelope signal is obtained by the combination of the modulated reflected chip harmonic and the external RF CW improving the harvesting efficiency.

The paper presents the first findings on the topic with the objective to demonstrate the proposed concept. Some additional efforts could be dedicated to the improvement of the integration technique of RFID and EEH sections by means of more accurate equivalent models of the diode and RFID chip, for instance: (i) in order to better exploit the HB tool and improve the device models, the experimental characterization of the devices used as inputs for the model should consider more harmonic frequencies; (ii) the use of CMOS diode-connected transistors to model the RFID chip rectifier could better reflect the RF operation occurring in the RFID chips.

Some future research paths could be addressed in the use of specific tuned frequencies for the RFID-TR, considering bands with great power density like broadcasting communication systems or frequencies belonging to the Industrial Scientific Medical (ISM) band. Further research efforts could be also dedicated to the combination of design methods such as the used in Class-E or Class-F rectifiers with the proposed composite rectifier method.

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REFERENCES

[1] Duroc, Y.; Kaddour, D.: RFID potential impacts and future evolution for green projects. Energy Procedia, **18** (2012), 91–98.

[2] De Koomey, J.G.; Berard, S.; Sanchez, M.; Wong, H.: Implications of historical trends in the electrical efficiency of computing. IEEE Ann. Hist. Comput., **33** (3) (2011), 46–54.

[3] Impinj. Monza R6 RFID Tag Chip. Optimized for Retail Environments. [Online]. Available: http://www.impinj.com/products/tag-chips/monza-r6/=opt

[4] De Donno, D.; Catarinucci, L.; Tarricone, L.: A battery-assisted sensor-enhanced RFID tag enabling heterogeneous wireless sensor networks. IEEE Sens. J., **14** (4) (2014), 1048–1055.

[5] Cook, B. et al.: RFID-based sensors for zero-power autonomous wireless sensor networks. IEEE Sens. J., IEEE, **14** (8) (2014), 2419–2431.

[6] Ramos, A.; Lazaro, A.; Girbau, D.: Semi-passive time-domain UWB RFID system. IEEE Trans. Microw. Theory Tech., **61** (4) (2013), 1700–1708.

[7] Athalye, A.; Savic, V.; Bolic, M.; Djuric, P.: Novel semi-passive RFID system for indoor localization. IEEE Sens. J., **13** (2) (2013), 528–537.

[8] Duroc, Y.; Andia Vera, G.: Towards autonomous wireless sensors: RFID and energy harvesting solutions, in Internet of Things. Springer, 2014,pp. 233–255.

[9] Georgiadis, A.; Collado, A.: Improving range of passive RFID tags utilizing energy harvesting and high efficiency class-E oscillators, in 2012 Sixth European Conf. on Antennas and Propagation, March 2012, 3455–3458.

[10] Costanzo, A.; Roselli, L.: EM- and piezo-scavengers: Two useful solutions in highly humanized scenarios toward a greener world, in 2012 IEEE MTT-S Int. Microwave Workshop Series on Innovative Wireless Power Transmission: Technologies, Systems, and Applications, May 2012, 15–18.

[11] Vaz, A. et al.: Full passive UHF tag with a temperature sensor suitable for human body temperature monitoring. IEEE Trans. Circuits Syst. II: Express Briefs, **57** (2) (2010), 95–99.

[12] Carvalho, N. et al.: Wireless power transmission: RD activities within Europe. IEEE Microw. Theory Tech. Trans., **62** (4) (2014), 1031–1045.

[13] Shinohara, N.: Recent wireless power transmission via microwave and millimeter-wave in Japan, in 2012 IEEE Microwave Conf. (EuMC), 42nd European, October 2015, 1347–1350.

[14] Popovic, Z.: Cut the cord: low-power far-field wireless powering. IEEE Microw. Mag., **14** (2) (2013), 55–62.

[15] Roberg, M.; Reveyrand, T.; Ramos, I.; Falkenstein, E.; Popovic, Z.: High-efficiency harmonically terminated diode and transistor rectifiers. IEEE Trans. Microw. Theory Tech., **60** (12) (2012), 4043–4052.

[16] Scheeler, R.; Korhummel, S.; Popovic, Z.: A dual-frequency ultralow-power efficient 0.5-g rectenna. IEEE Microw. Mag., **15** (1) (2014), 109–114.

[17] Georgiadis, A.; Andia, G.; Collado, A.: Rectenna design and optimization using reciprocity theory and harmonic balance analysis for electromagnetic (EM) energy harvesting. IEEE Antennas Wireless Propag. Lett., **9** (2010), 444–446.

[18] Andia Vera, G.; Duroc, Y.; Tedjini, S.: Analysis of harmonics in UHF RFID signals. IEEE Trans. Microw. Theory Tech., **61** (6) (2013), 2481–2490.

[19] Ladan, S.; Wu, K.: 35 GHz harmonic harvesting rectifier for wireless power transmission, in 2014 IEEE MTT-S Int. Microwave Symp. Digest, June 2014, 1–3.

[20] Andia Vera, G.; Duroc, Y.; Tedjini, S.: RFID test platform: nonlinear characterization. IEEE Trans. Instrum. Meas., **63** (9) (2014), 2299–2305.

[21] Boaventura, A.; Carvalho, N.: Maximizing dc power in energy harvesting circuits using multisine excitation, in 2011 IEEE MTT-S Int. Microwave Symp. Digest, June 2011, 1–4.

[22] Trotter, M.; Griffin, J.; Durgin, G.: Power-optimized waveforms for improving the range and reliability of RFID systems, in 2009 IEEE Int. Conf. on RFID, April 2009, 80–87.

[23] Collado, A.; Georgiadis, A.: Improving wireless power transmission efficiency using chaotic waveforms, in 2012 IEEE MTT-S Int. Microwave Symp. Digest, June 2012, 1–3.

[24] Collado, A.; Georgiadis, A.: Optimal waveforms for efficient wireless power transmission. IEEE Microw. Wireless Compon. Lett., **24** (5) (2014), 354–356.

[25] E. M. M. SA. Em4325 datasheet. [Online]. Available: http://www.emmicroelectronic.com=opt

[26] Zheng, Y.C.; Hua, Zheng, Y.L.; Hong, W.: Design of a miniaturized RFID tag antenna with BAP technique, in 2014 3rd Asia-Pacific Conf. on Antennas and Propagation, July 2014, 256–258.

[27] A. Technologies. Hsms-286x series. [Online]. Available: http://www.avagotech.com/docs/AV02-1388EN=opt

[28] Hagerty, J.A.: Nonlinear Circuits and Antennas for Microwave Energy Conversion. Ph.D. thesis, Department of Electrical and Computer Engineering, University of Colorado, 2003.

[29] Andia Vera, G.; Georgiadis, A.; Duroc, Y.; Tedjini, S.: Cooperative Integration of Harvesting Sections for Passive RFID Communication, in 2015 IEEE MTT-S Int. Microwave Symp. Digest (to be presented), May 2015, 1–3.

[30] Yoo, T.W.; Kain, C.: Theoretical and experimental development of 10 and 35 GHz rectennas. IEEE Trans. Microw. Theory Tech., **40** (6) (1992), 1259–1266.

[31] Valenta, C.; Durgin, G.: Rectenna performance under power-optimized waveform excitation, in 2013 IEEE Int. Conf. on RFID, April 2013, 237–244.

[32] Ladan, S.; Ghassemi, N.; Ghiotto, A.; Wu, K.: Highly efficient compact rectenna for wireless energy harvesting application. IEEE Microw. Mag., **14** (1) (2013), 117–122.

[33] De Vita, G.; Iannaccone, G.: Design criteria for the RF section of UHF and microwave passive rfid transponders. IEEE Trans. Microw. Theory Tech., **53** (9) (2005), 2978–2990.

[34] Liu, J.: Dual-band RFID tag antenna using coplanar inverted-f/l structure, in 2010 IEEE Int. Conf. on RFID-Technology and Applications, June 2010, 96–99.

[35] Marrocco, G.: The art of UHF RFID antenna design: impedance-matching and size-reduction techniques. IEEE Antennas Propag. Mag., **50** (1) (2008), 66–79.

[36] Nguyen, D.S.; Le, X.C.; Pham, T.T.; Nguyen, V.H.; Dang, M.C.; Tedjini, S.: Novel design of RFID UHF passive tag for wideband applications by direct and contactless chip connection, in 2012 IEEE Int. Conf. on RFID-Technologies and Applications, November 2012, 131–136.

[37] Andia Vera, G.; Nawale, S.D.; Duroc, Y.; Tedjini, S.: Optimum integration of passive UHF RFID tag-rectenna in a single feed dual band antenna, in 2014 XXXIth URSI General Assembly and Scientific Symp., August 2014, 1–4.

[38] Rao, K.; Nikitin, P.; Lam, S.: Antenna design for UHF RFID tags: a review and a practical application. IEEE Trans. Antennas Propag., **53** (12) (2005), 3870–3876.

[39] Impinj. Speedway Readers. [Online]. Available: http://www.impinj.com/products/readers/

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