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RESEARCH ARTICLE

Harmonically terminated high-power rectifier for wireless power transfer

AASRITH GANTI[1,2], JENSHAN LIN[2], RAUL A. CHINGA[3] AND SHUHEI YOSHIDA[4]

The paper presents a simplified analysis of harmonically terminated rectifier circuit and experimental results of a Schottky diode rectifier with even and odd harmonic terminations. The analysis is based on the Fourier series expansion of the voltage and current across the diode circuit. Harmonic terminations similar to the techniques used for power amplifiers are studied. A maximum efficiency of 84% at 30 dBm is obtained with second- and third-order harmonics terminated. The optimum value of dc load to maximize efficiency is obtained by sweeping the load. An optimal operating range of 28–35 dBm is obtained. The applications of the rectifier in wireless charging and power transfer systems are discussed.

Keywords: Wireless power, Rectifier, Harmonically terminated, High efficiency high power rectifier

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I. INTRODUCTION

Nikola Tesla first experimented with wireless power in 1891, but it gained momentum and widespread interest in the 1970s [1]. During this time, the very first high-efficiency rectenna, a combination of antenna and rectifier circuit used to rectify the incoming ac signal, was implemented [2–4]. Designs during this era constituted far-field solutions that have applications in military, space, and industries. Wireless power transfer can be categorized into three types: near-field transfer, microwave power transfer, and microwave power harvesting; among which, near-field transfer can deliver tens of watts of power using magnetic field coupling with less safety concerns and with higher efficiency. Thus, this design is aimed for near-field high-power applications. The power levels under consideration may cause interference to the large wireless traffic present at higher frequencies [5]. Therefore, 13.56 MHz is chosen as the frequency of operation.

In a radio frequency (RF) wireless power receiver, the rectifier circuit is a major contributor to the overall loss of efficiency. The RF wireless power receiver system has a receiving antenna followed by a filter-rectifier circuit to convert energy from the transmitted RF signal. Ideally, the switch used in the circuit should have no resistance, but in practice the diode used as a switch has parasitic resistance, resulting in a lower efficiency. To minimize this loss in efficiency, we describe a technique to engineer waveforms as used in switch mode power amplifiers [6] in this paper.

Yoshida *et al.* [7] demonstrated a high-efficiency rectifier by terminating the second-harmonic component using a series-resonant circuit. A maximum efficiency of 85% was reached at 27 dBm, but the efficiency dropped with an increase in the input power; falling to 60% at 33 dBm. Fu *et al.* [8] designed a wireless power system at 13.56 MHz that uses a full-wave rectifier with an efficiency of 76–81%. A high-power, high-efficiency rectifier designed by Liou *et al.* [9] uses series and parallel power division circuit to increase conversion efficiency at high-power levels. Efficiencies of 62 and 76% have been shown for the series and parallel power divider networks, respectively. Hosain and Kouzani [10] compared several rectifier configurations to operate at 30 dBm, but none of which has an efficiency of more than 75%. Noda and Shinoda [11] used Schottky diodes in an anti-symmetric configuration to operate in Class-F configuration, achieving 78% efficiency at 27 dBm. Falkenstein *et al.* published a rectifier design at 2.14 GHz using a modified inverse Class-F GaN power amplifier that approached 85% conversion efficiency at 40 dBm [12]. Kang *et al.*, discussed the implementation of a high-efficiency rectifier [13]. To achieve a high-efficiency, these designs sacrifice simplicity and ease of implementation. Several high-efficiency rectifiers have been discussed in literature, but they are low-power rectifiers operating at higher frequencies.

The novelty of the solution presented in this paper lies in the design of a robust, low-frequency, high-power rectifier for wireless charging at 1 W level. To achieve high conversion efficiency, implementation of harmonic terminations in a shunt diode rectifier is presented. The theory based on Fourier analysis as well as the design and measurment results of our existing prototype are discussed in the sections that follow.

[1]Philips Healthcare, 3545 47th Avenue, Gainesville, Florida 32608, USA
[2]Department of Electrical and Computer Engineering, University of Florida, Gainesville, Florida, USA
[3]Space Systems Loral, Palo Alto, California, USA
[4]Radio Application, Guidance and Electro-Optics Div., Integrated Undersea Warfare Systems Development and Promotion Program, NEC Corporation, Tsukuba, Japan
Corresponding author:
A. Ganti
Email: aasrith.ganti@philips.com

II. BASIC ARCHITECTURE AND FOURIER ANALYSIS

As shown in Fig. 1, the receiver chain consists of an input matching network, a switching device, harmonic terminations, an output matching circuit, and a dc load. In practice, switching elements are implemented using semiconductor devices such as transistors and diodes [12]. The harmonics in the receiver circuit are analyzed by applying Fourier series expansion. Under ideal conditions, the diode behaves as a switch with resistance given by (1).

$$R_d = \begin{cases} 0, & \text{diode is ON,} \\ \infty, & \text{diode is OFF.} \end{cases} \tag{1}$$

The input RF signal is represented by (2).

$$V_i = V_m \sin(\omega t). \tag{2}$$

The response of the diode connected in a shunt reverse bias configuration is represented in (3). Fourier series expansion, as explained in [6, 12] is applied to study the harmonics generated in the circuit. The transformed equations for voltage across and current through the diode are derived as (4) and (5).

$$V_d = \begin{cases} V_m \sin(\omega t), & 0 \le t \le \pi, \\ 0, & \pi \le t \le 2\pi, \end{cases} \tag{3}$$

$$v_d = V_{dc} + V_1 \cos(\omega t) + V_2 \cos(2\omega t) + V_3 \cos(3\omega t), \tag{4}$$

$$i_d = I_{dc} + I_1 \cos(\omega t) + I_2 \cos(2\omega t) + I_3 \cos(3\omega t). \tag{5}$$

Voltage and current waveforms contain high-frequency harmonics that can be shaped to achieve high RF–dc conversion efficiencies. The diode's internal resistance is the main cause of power loss. However, tuned circuits can be used to terminate high frequency to shape voltage and current, forcing a zero voltage switching condition across the diode. In this paper, Class-F type of terminations is implemented where all the odd harmonic components are open-circuited and even harmonic components are short-circuited. Terminations are designed using discrete components unlike in [11, 12] where transmission lines were used. Transmission lines at 13.56 MHz would physically be too long, making the design inefficient and impractical.

The terminations work on the concept of different impedance values seen by the harmonics. For odd harmonic terminations, a parallel LC tank, which has a reflection coefficient of one (Fig. 2(a)) is used. The circuit presents high impedance to the odd harmonic of voltage (V_{odd}) and reflects the signal toward the diode. Since a high impedance is present at the odd harmonics (Z_{odd}), Ohm's law ($V_{odd} = Z_{odd} \times I_{odd}$) results in an infinitesimal current at odd harmonics (I_{odd}). Thus, the odd harmonic component of current is ideally reduced to zero.

The even-order harmonic termination circuit, represented by Fig. 2(b) creates low impedance and a reflection coefficient of -1 to even harmonics. Since impedance seen by even harmonic components (Z_{even}) is ideally zero, Ohm's law ($V_{even} = Z_{even} \times I_{even}$) results in a zero even-order harmonic components (V_{even}) and reflects even harmonic component of current (I_{even}).

The reflection coefficients measured across the tuned circuits in the prototype are presented in Smith charts simulated using Agilent ADS. From Fig. 2 it is clear that for the third-harmonic frequency component, i.e. 40.68 MHz, the reflection coefficient is 1 (open circuit) and for the second-harmonic frequency component, i.e. 27.12 MHz, the reflection coefficient is -1 (short circuit). Therefore, the terminations are pivotal for controlling impedance of each of the harmonics to shape the voltage and current across the diode.

For obtaining a zero loss condition as shown in Fig. 3, all the harmonic frequency components need to be terminated. The phenomenon of waveform shaping using termination circuits is shown in this figure. Figure 4 illustrates the effect of terminations on the voltage and current waveforms across the diode when the finite numbers of harmonics are terminated. When no harmonic terminations are used, the circuit behaves like a half-wave rectifier. If only one termination is used, then the efficiency of the circuit is greater than that of the half-wave rectifier, but still does not reach an appreciable level. The circuit attains optimum efficiency when both second-

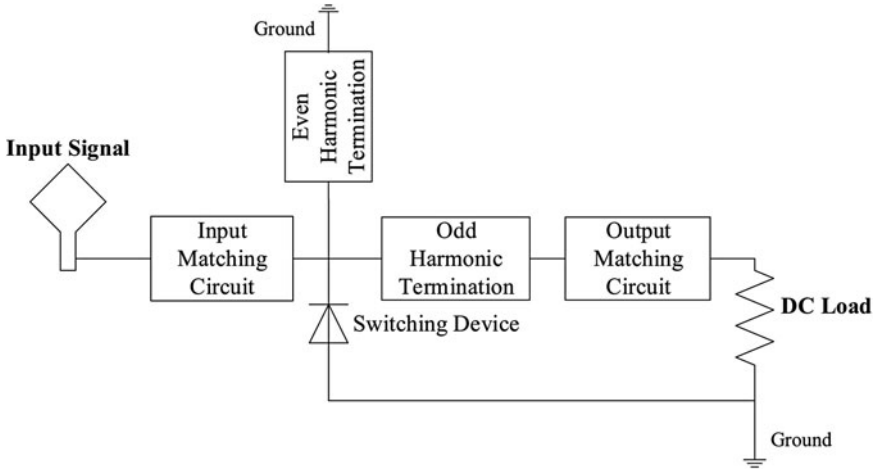

Fig. 1. Block diagram of a WPT receiver system.

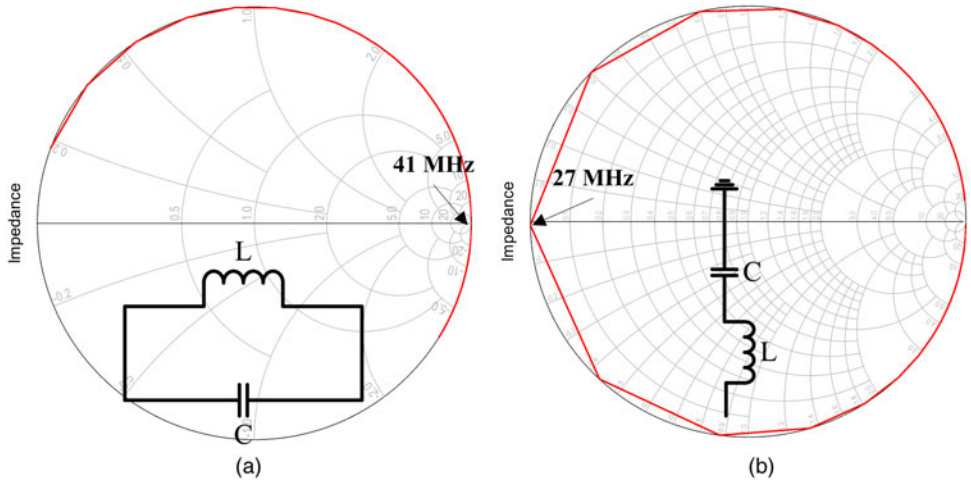

Fig. 2. (a) Third-order harmonic termination circuit (b) Second-order harmonic termination circuit.

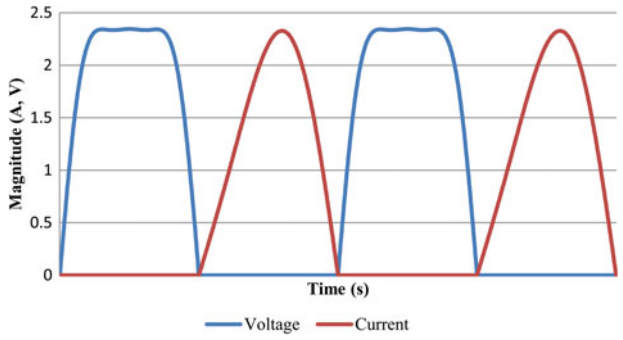

Fig. 3. Ideal voltage and current waveforms across the diode if all harmonics are terminated.

and third-order harmonics are terminated. As shown in Fig. 5, if higher-order harmonics are terminated, the voltage current waveforms across the diode approaches the theoretical prediction, but the dc resistance (DCR) of the higher-order harmonic termination circuit will cause additional loss in efficiency. Moreover, the design complexity outweighs the benefits of using higher-order terminations. So, only second- and third-harmonic terminations are considered for practical implementation and prototyping.

Applying this approximation to equations (4) and (5), the voltage and current across the diode are now given by (6) and (7).

$$v_d = V_{dc} + V_1 \cos(\omega t) + V_3 \cos(3\omega t), \tag{6}$$

$$i_d = I_{dc} + I_1 \cos(\omega t) + I_2 \cos(2\omega t). \tag{7}$$

III. EXPERIMENT

Simulations in ADS and bench tests on a shunt diode rectifier with second- and third-order harmonics terminated are performed to validate the theory discussed. The terminations built using lumped components are tuned to 27.12 and 40.68 MHz, the second- and third-harmonic frequencies,

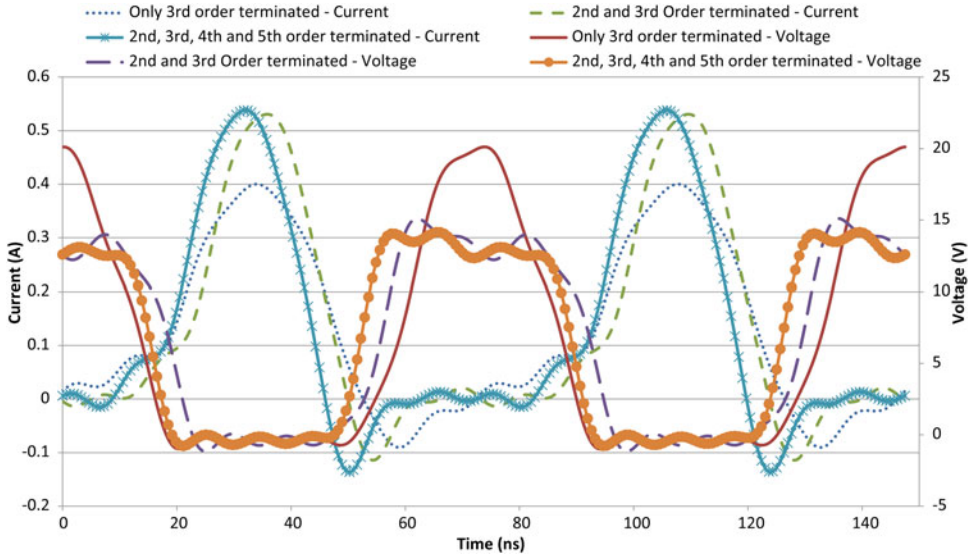

Fig. 4. Voltage and current waveforms across the diode when different terminations are used.

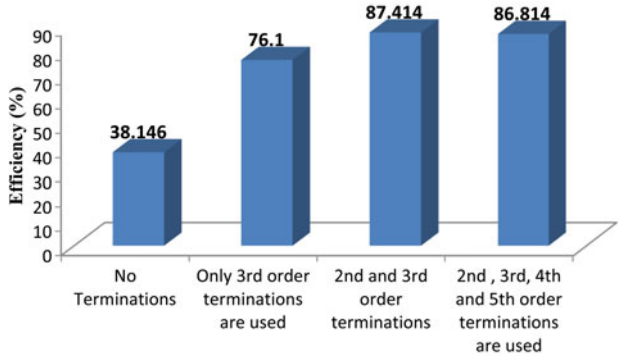

Fig. 5. Comparison of efficiency with number of terminations being used.

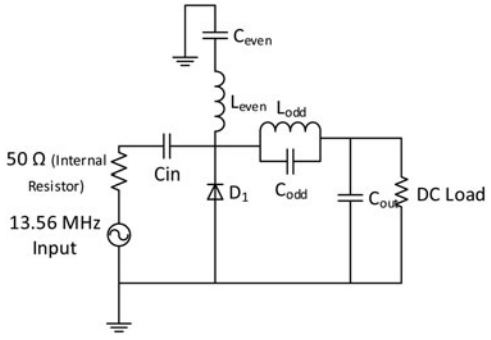

Fig. 6. Schematic representation of the rectifier circuit.

respectively. MBRA 140, is chosen as the switching device for this work, as it has a high reverse breakdown voltage (40 V), large current-handling capabilities (1 A) and a low forward voltage drop (0.55 V) (see the Appendix). The junction capacitance and resistance of this device are ∼40 pF and ∼98 mΩ, respectively. C_{in} and C_{out} form the input and output match circuits, respectively. Their values are chosen to create a power match at the source, reducing any mismatch loss. The value of C_{out}, part of the smoothing circuit, ensures that the RC time constant of the circuit is $> 1/f\,(\tau = R_{load} \times C_{out} \gg 1/f)$. Figure 6 shows the schematic representation of the rectifier and Table 1 lists the components used for the

Table 1. Components.

Schematic label	PCB label	Value
C_{even}	C_{even}	22.7 pF
L_{even}	L_{even}	1.8 μH
C_{odd}	C_{odd}	10 pF
L_{odd}	L_{odd}	1.4 μH
Schottky diode (D_1)	Schottky diode (D_1)	MBRA 140
C_{in}	L_1	2200 pF
C_{out}	C_{out}	2200 pF
	L_{choke}, C_1, C_2	(Not used)

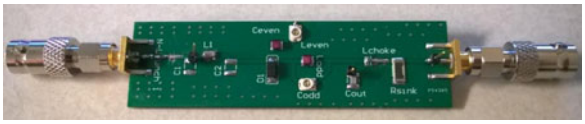

Fig. 7. Experimental board.

tests performed. Simulations in ADS use the Harmonic Balance solver with the fundamental frequency set to 13.56 MHz and the order set to 7. To increase the computational accuracy of the solver, the order is set to 7 even though only 5 harmonics are analyzed. Figures 7 and 8 show the populated PCB and measurement system used to perform bench tests.

To prove the Class-F operation of this design, the load used at the output to measure voltage and currents across the diode is chosen based on simulations in ADS. It is observed that a large output impedance causes a high reverse voltage to appear across the diode, which results in a large output dc voltage. A larger load results in higher efficiency, but the diode reaches breakdown faster [14]. The circuit is simulated with several loads and the efficiencies are measured between 0 to 50 dBm. A 100 Ω load is chosen as it is a good compromise between, achieving high-efficiency and preventing the diode from reaching breakdown faster. The simulated load analysis is plotted in Fig. 9.

The effect of terminations is verified by analyzing voltage and current across the diode. The ratio of output dc power to the input RF power determines the conversion efficiency

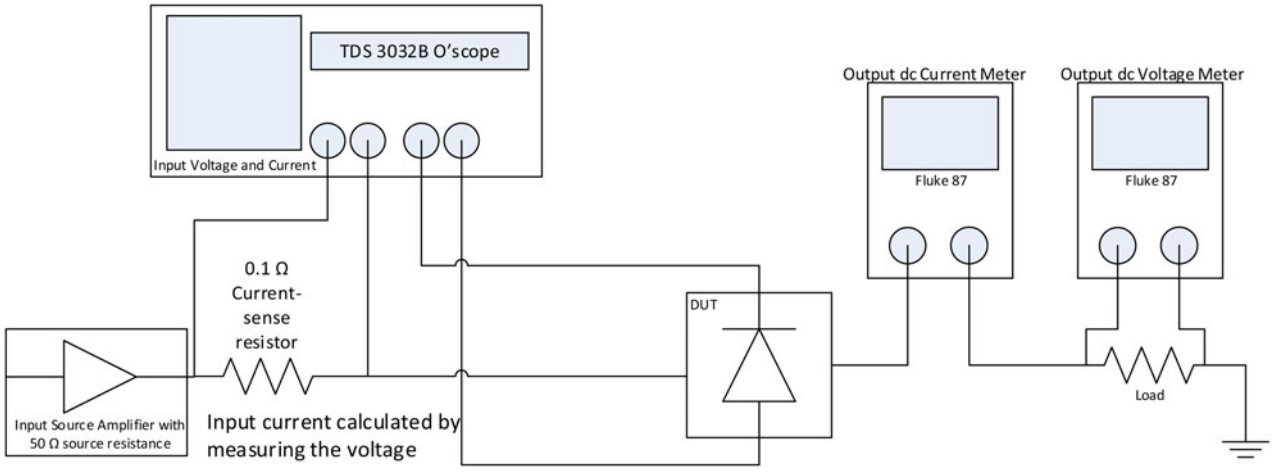

Fig. 8. Measurement system.

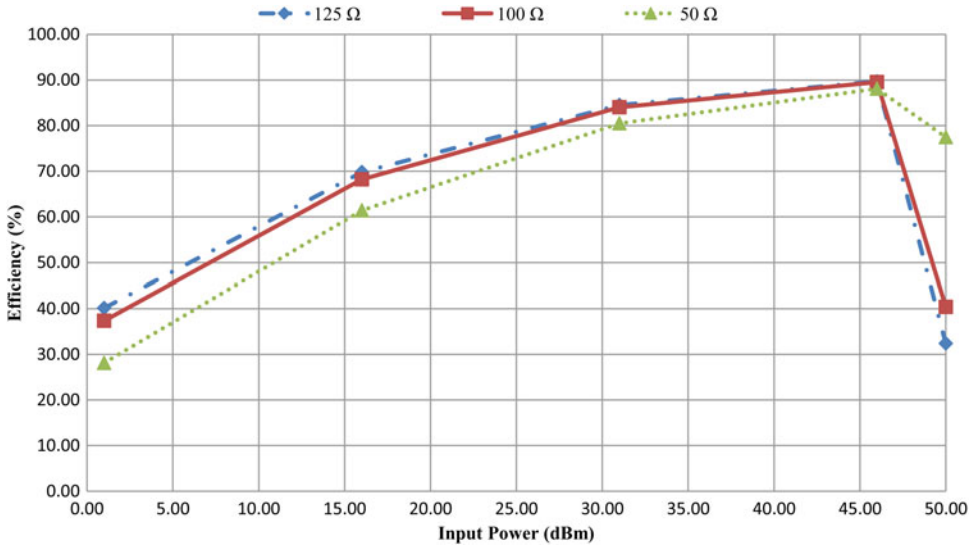

Fig. 9. Simulated output versus dc load.

(η = output dc power/input RF power). From Fig. 10, it is seen that the simulation and the bench test results are in agreement of each other. The square voltage and sinusoidal current waveforms, confirm the use of terminations to improve the efficiency of the rectifier. It is seen that the measured waveforms are non-ideal representations of the Class-F waveforms. This could be an effect of the voltage reduced by the junction capacitance, C_j, of the diode which is similarly explained by Guo *et al.* [14] in their analysis.

The efficiency of the circuit at different power levels is presented in Fig. 11. This graph represents the typical behavior of a harmonically terminated diode rectifier. The entire plot can be divided into three regions based on the operating point of the diode; the first being the "turn-on" region where the input power is not sufficient to completely turn ON the diode. This results in a large power loss across the diode. In the second region, the diode is ON and is operating nominally; this is also the region where the maximum rectification efficiency is obtained. Beyond this region, if a higher input power is applied, the diode enters breakdown region and may lead to device failure [14].

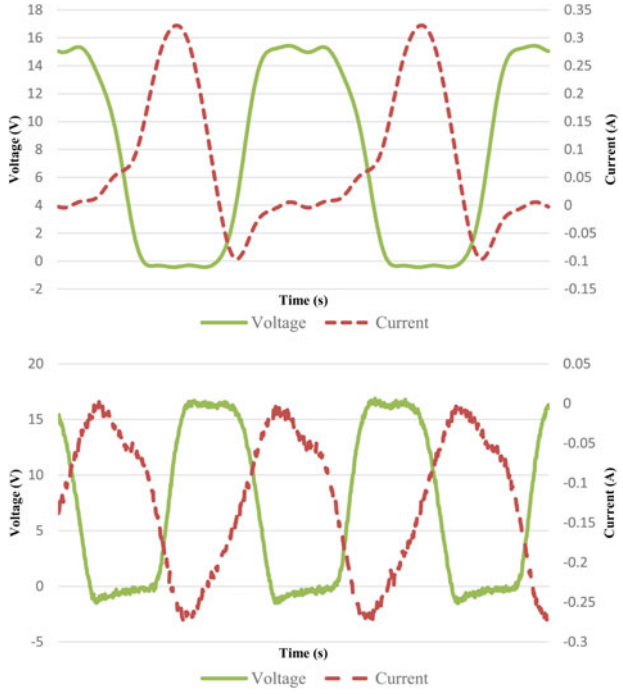

Fig. 10. Simulated (top) and measured (bottom) voltage and current across the diode.

In our design, a maximum efficiency of 84.3% is obtained with a 30 dBm input. Also, for the input power ranging from 28 to 35 dBm, the average conversion efficiency is 80%. Beyond which the diode starts entering the breakdown region. Figure 12 represents the power budget of this design. As explained in the introduction, most losses occur at the diode. However, the deviation in the measured and simulation results are attributed to DCR losses present in the lumped components. Since low frequencies are being used, the dielectric losses in the substrate can be neglected. In this work, either the electrostatic resistance (ESR) or DCR in capacitors and inductors are the main contributors for the loss in rectification efficiency.

There are ways in which the measured results can be improved. First, the efficiency can be brought closer to the simulation results by choosing low tolerance components and components with low parasitic losses. Second, a diode with lower turn ON voltage, lower Rd, and lower junction capacitance [14] can be chosen.

Rectifier designs discussed in literature are listed in Table 2. Kang *et al.* [13] developed a Schottky diode rectifier where a control circuit is used to switch between rectifier and voltage multiplier modes. An impedance matching controller is also implemented to match varying loads. Although a higher conversion efficiency is achieved, a complex architecture is needed. The highest conversion efficiency at 40 dBm is reported by Roberg *et al.* [12]. However, this design is implemented using a GaN transistor at a higher frequency with transmission line harmonic terminations. Our design has an advantage over these designs by being simpler to implement and has the highest efficiency at the frequency of operation.

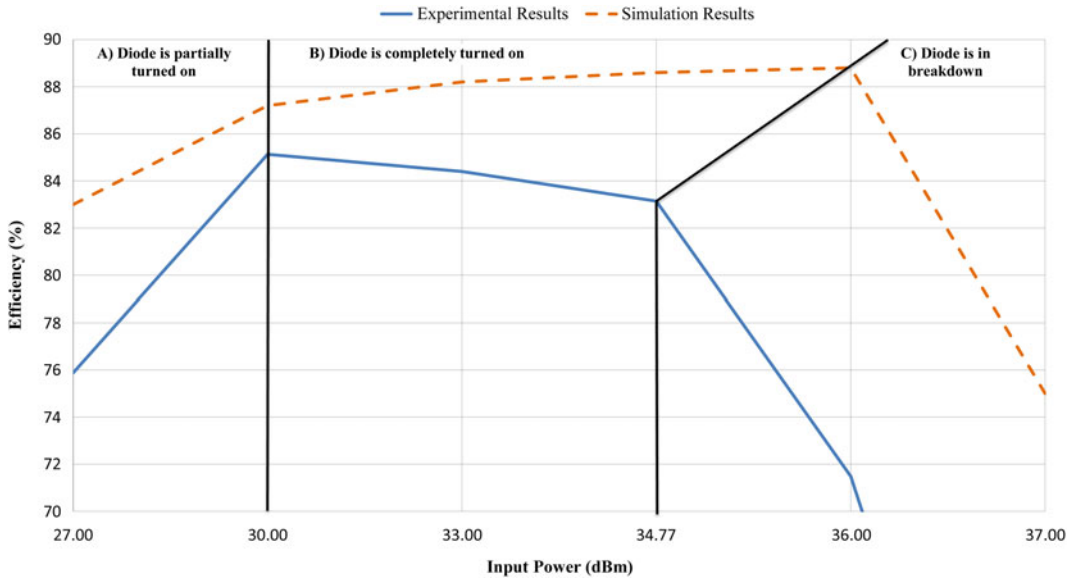

Fig. 11. Efficiency comparison of experimental and simulated data.

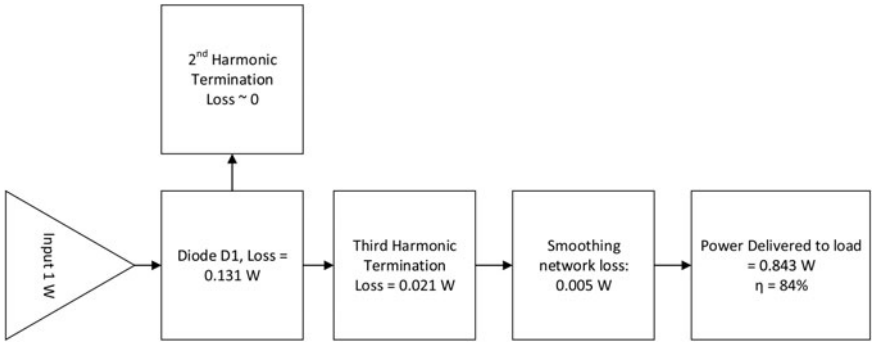

Fig. 12. Power budget diagram.

Table 2. Comparison of rectifier circuits.

Paper	Frequency of operation	Power (dBm)	Method used to increase efficiency	Efficiency achieved (%)
[13]	128 kHz	36	Schottky diode with control circuit	85
[7]	13.56 MHz	30	Schottky second-order terminations	75
[8]	13.56 MHz	46	SiC diodes in Full-wave configuration	78
This work	13.56 MHz	30	Schottky diode with even and odd terminations	84
[10]	915 MHz	30	Schottky diode in various configurations	75
[9]	920 MHz	41	Schottky diodes with Power Split circuits	62–76
[12]	2.14 GHz	40	GaN transistor in Class F^{-1}	85
[11]	2.45 GHz	27	Full-wave with third order	77.9
[15]	2.45 GHz	16	Schottky second and third-order terminations	66.5

IV. CONCLUSION

We have developed a high-efficiency, low-complexity rectifier geared toward short-range wireless power transfer. Such a device will enable fast and efficient charging of devices requiring high power. This will enable wireless charging for not only portable electronic devices, but also for larger devices such as laptops. The flexible design of the rectifier allows it to be customized for use in various wireless power receiver systems.

The rectifier based on a shunt Schottky diode with harmonic terminations is simulated and tested with input power ranging from 27 to 40 dBm. On comparison with similar devices in literature, our design achieves a power efficiency of 84%, which is higher than most shown in Table 2. The highest reported efficiency of 85% in Table 2 comes at the expense of greater design complexity and higher implementation cost than our prototype. Furthermore, the efficiency of our

design can readily be improved, if needed, using Schottky diodes with lower junction capacitance and forward voltage, and components with smaller tolerance, ESR and DCR.

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None.

STATEMENT OF INTEREST

None.

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Aasrith Ganti received his B.S. in Electronics and Communication Engineering from the JNT University in 2008 and M.S. in Electrical Engineering in 2014. Presently he is a part of the development team at Philips Healthcare. His main research interests are wireless power transfer, energy harvesting, and semiconductor devices.

Jenshan Lin received the Ph.D. degree in Electrical Engineering from the University of California at Los Angeles (UCLA), Los Angeles, CA, USA, in 1994. He was with AT&T Bell Laboratories (which later became Lucent Bell Labs), Murray Hill, NJ, USA, from 1994 to 2001, and its spin-off Agere Systems from 2001 to 2003. In July 2003, he joined the University of Florida, Gainesville, FL, USA, as an Associate Professor and became a Professor in August 2007. He has authored or co-authored over 250 technical publications in refereed journals and conferences proceedings, and holds 14 US patents. His research interests include sensors and biomedical applications of microwave and millimeter-wave technologies, wireless power transfer, RF-integrated circuits, and antennas. He is a Fellow of IEEE and currently serves as the Editor-in-Chief of IEEE Transactions on Microwave Theory and Techniques for the term of 2014–2016.

Raul A. Chinga received his B.S. and Ph.D. degrees from the University of Florida in 2008 and 2013, respectively. His dissertation work concentrated on high efficient power amplifiers for DBD plasma generation for sterilization applications. In addition, he concentrated on wireless power transfer systems via inductive coupling for near field and midrange applications. During his time at the University of Florida, he was awarded the Bridge to the Doctorate Fellowship in 2008, the Graduate Research Fellowship Honorable Mention award by NSF in 2010, and the Varosi Scholarship in 2012. His is currently working at Space Systems Loral in Palo Alto, California, working on various aspects of the spacecraft power system.

Shuhei Yoshida received his M.S. degree from Keio University, Japan in 2007. His dissertation work concentrated on high efficient wireless power transfer systems and its applications. He is currently working at NEC Corporation in Japan, working on various aspects of the wireless power transfer system.

APPENDIX

Table 3. Spice model for MBRA140.

Parameter	Value	Unit
I_s	4.21144×10^{-7}	A
R_s	0.098312	Ω
N	0.973949	
C_{jo}	$1.4486 \times 10^{-10}10$	F
V_j	1.09761	V
M	0.536808	
Fc	0.5	
B_v	40	V
Ibv	0.0005	A
Nbv	0.973949	
Kf	0	
Af	1	
$Tnom$	27	C
Xti	2.44859	
E_g	0.596398	eV