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Harmonic distortion considerations for an integrated WPT-PLC system

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Abstract

This paper presents design considerations for an integrated wireless power transfer (WPT) and power line communication (PLC) system (e.g. WPT-PLC). The main goal is to enable wireless charging of mobile electronic products, along with high data rate communication over the shared wireless inductive resonant channel. Starting from a couple of resonant coils, characterized by the *S*-parameters matrix, the design of an impedance matching network and decoupling filters is carried out to better decouple power and data signals. A pulse-driven class-E power amplifier (PA) and a rectifier are first conceived based on the measured *S*-parameters and load-pull characterizations. Second, a sine-driven class-E power link, operating at 6.78 MHz, is proposed to reduce the total harmonic distortion of the integrated WPT-PLC system. These design steps aim to ensure high-power efficiency and low harmonic distortion of the class-E PA in order to mildly affect the channel capacity of the PLC. The harmonic interferences of the pulse-driven and sine-driven class-E power links are compared and discussed, together with the electromagnetic compatibility levels, the channel capacity, and the noise disturbances of the PLC channel in order to guarantee an optimized power and data transfer in the integrated WPT-PLC system.

Introduction

Wireless power transfer (WPT) technology is nowadays one of the leading research topics, with large foreseen investments at the industrial level. Its applications can range from low power transfer (e.g. 5 W) for wearable products such as smart phones and watches, to high-power (e.g. 20 W to 100 kW) wireless charging of consumer electronics device such as laptops, domestic robots up to e-bikes and electric vehicles (EVs) [1–5].

At the same time, the rise of renewable energy generators and the development of the smart grid have created the need of constant information exchange between different components of a power infrastructure. The constant increasing diffusion of battery-enabled devices and machines is an additional boost to this situation [1–6]. In the last decade, power line communication (PLC) technology has gained new life establishing itself as the easiest way to implement the abovementioned communication in power grids [4–6], and to enable sensor cloud-based control in industrial or domestic electronic applications [6].

The recent development of the Home Plug Green PHY protocol (specifically dedicated to EVs) shows the future trend, and that communication speeds of hundreds of Mbits per second can be reached [7–10].

Recently, the authors proposed a WPT-PLC system that integrates these two technologies [11–15], showing its capability to guarantee an efficient power transfer and broadband data communication through the wireless inductive channel. However, the channel capacity of the communication link of the WPT-PLC system was simply evaluated assuming additive white Gaussian noise (AWGN) at the receiver.

Switching mode class-E power amplifier (PA), driven between the cut-off and the saturation modes (i.e. ON/OFF switch) by a pulse width modulated (PWM) signal [16–22], is a commonly chosen power efficient and cost effective design structure for WPT transmitters; in particular, one of the most high power effective transistor solution for WPT design is the gallium nitride (GaN) technology. At the same time, a class-E PA operates in a highly non-linear regime, therefore it generates a distorted output signal at the transmitting and receiving coils' terminals, which represent the shared channel for power and information signals. As a matter of fact, this is usually the design compromise that the wireless power link designer is facing for biasing and selecting the adequate PA class that balances the trade-off between linearity and distortion [23, 24].

In addition, the power link creates electromagnetic interference disturbing not only the PLC operation, but also electronic appliances embedded in the device under charge as well as other devices connected to the power grid. Moreover, the performances of the transceivers need to conform to industry standards and meet strict electromagnetic compatibility (EMC)

criteria [25, 26]. In this paper, the harmonic distortions generated by the high-power WPT link are estimated and analyzed in order to assess their impact on the PLC channel capacity. Furthermore, guidelines for the proper design of such combined system are outlined.

The main contributions of this work are as follows:

- this study is the first attempt to design a PA for a combined WPT-PLC system, studying the feasibility and providing the guidelines for the realization;
- pulse-driven and sine-driven class-E power links are compared and discussed;
- this study also represents the first attempt to assess the impact of the harmonics produced by the PA on the PLC channel;
- the designs discussed in this paper are all based on measurements of the channel frequency response of a realized WPT-PLC link.

The paper is organized as follows: "Analysis and design of the WPT-PLC system" section describes the design and optimization steps of the impedance matching network (IMN) for minimizing the harmonic distortions. The load-pull design step of the IMN is aimed at maximizing the power efficiency of the power link, while reducing the variation of the delivered output power facing different loading conditions. "PLC and WPT integration validation" section presents a comparative analysis of the harmonic distortions between pulse-driven and sine-driven class-E power link in the integrated WPT-PLC system. In addition, the effects of the sine-driven class-E power link interferences on the capacity of the PLC channel are assessed according to the recent EMC classifications and regulations [25, 27]. Finally, conclusions are drawn in the "Conclusion" section.

Analysis and design of the WPT-PLC system

System description and parameters' definition

The block diagram illustrating the main components of the integrated WPT-PLC is shown in Fig. 1. The inductive channel is composed of the transmitting (Tx) and receiving (Rx) coils (with self-inductances L_T and L_R respectively), which are separated by the distance d and characterized by a coupling factor $k = M/\sqrt{L_T L_R}$, in which M is the mutual inductance coefficient. The whole design procedure of the PA is applied to the first prototype of the system built by the authors ([11], also shown in Fig. 2) and designed to work in the ISM frequency band (resonant frequency $f_0 = 6.78$ MHz).

The Spice circuit schematic of the class-E PA and rectifier is shown in Fig. 3. The power link model consists of a dc supply V_{dd}, a finite-dc feed inductor L_d, the Spice models for the transistor and diode, a shunt capacitor C_1, a series resonant circuit $L_0 - C_0$, the inductors L_T and L_R, and the resistor R_L [16 17]. The capacitors C_T and C_R are inserted in the power link in order to create a resonant inductive channel at $f_0 = 6.78$ MHz $\left(\omega_0 \cong 1/\sqrt{C_T L_T} = 1/\sqrt{C_R L_R}\right)$ as it is usual in WPT systems, while the high pass (HP) filters are fabricated as described in [11] to decouple the interference between the power and data signals. The class-E PA transmitter efficiency η_T and the end-to-end efficiency η_{ee}, are defined as follows:

$$\begin{cases} \eta_T = \dfrac{P_T}{P_{dc}} = \dfrac{P_T}{P_T + P_{diss}} \\ \eta_{ee} = \dfrac{P_L}{P_{dc}} \end{cases} \tag{1}$$

where P_T is the transmitted output power, P_{dc} is the dc power supply, P_L is the power at the load, and P_{diss} is the power dissipated on the resistances of the circuit. A good design of the IMN shall minimize the time overlap between voltage and current waveforms to avoid power dissipation in the transistor, leading to maximum power efficiency [23, 24, 28–30].

The series $L_0 - C_0$ circuit is tuned to resonate at $f_0 = 6.78$ MHz, consequently it behaves as a short circuit at the fundamental frequency f_0 and as a high impedance branch at higher harmonic frequencies (e.g. $2f_0$ and $3f_0$, etc.). The loaded quality factor Q_L should be high enough to provide the required harmonic suppression: $C_0 = 1/(\omega_0 R_L Q_L)$ and $L_0 = 1/(C_0 \omega_0^2)$ [23].

We define $Z_{in,c}$ (see Fig. 3) as the impedance seen from the input point of the resonating system, consisting of coils and capacitors. The IMN will be placed before this point, with the aim of adapting the impedance seen by the PA, as shown in Fig. 4. Consequently we can define $Z_{in,m}$ as the impedance seen from the input of the matching network (see the blue dashed vertical line in Fig. 4).

The following sections describe the IMN design strategy, which aims at satisfying low harmonic distortions, high efficiency, and high-power transfer to the load. First, the capability of the IMN (designed for the power link) along with the HP filters (designed for the data link) is assessed, with the aim of matching the PA impedance and reducing the second and third harmonics of the high-power signal. Second, the load-pull design of the combined WPT-PLC system is carried out to further optimize the IMN, leading to reduced high-power variations in front of a wide range of loading and coupling conditions. The simulations are carried out by the harmonic balance in Advanced Design System from Keysight [31].

Low harmonic design

The enhanced mode high-electron-mobility GaN (eGaN) FET EPC2007C [32] transistor technology is preferred for the class-E PA design: it is characterized by low gate resistance R_G and low input capacitance C_{GS}, which reduces the power requirements of the pulse gate driver circuit. The absolute maximum ratings of the electrical characteristics of the EPC2007C eGaN are described in Table 1 [30] and the parasitic components are shown in Fig. 5.

As far as comparable MOSFETs, the EPC2007C offers significantly lower values of the input, output, and reverse transfer capacitances and inductance, with zero reverse recovery charge (Q_{RR}) in a smaller footprint for a given $R_{DS(ON)}$ [30, 32]. The time-constant associated with trapping effects in the eGaN device are included in our simulations to account for $R_{DS(ON)}$ variation which increases proportionally to the logarithm of the stress time.

The class-E rectifier circuit consists of a high voltage STPS5H100 Schottky diode from STMicroelectronics as a switching device and its Spice model can be easily obtained [32, 33]. The two high-Q coils (i.e. L_T and L_R) shown in Fig. 2 were designed and fabricated by the authors [11, 12] and the resonant inductive WPT channel was characterized, for different separating distances, using a vector network analyzer (VNA). The measured S_{21} parameters, under 10 Ω input/output loading conditions, are shown in Fig. 6; the maximum value of the transmission coefficient S_{21} is achieved at 6.78 MHz by design. The simulation results of the S-parameter characterization data of the fabricated two-coil channel show that the best inductive channel efficiency is achieved at the resonant frequency under 10 Ω I/O loading conditions. It is worth noting that the resonant channel profile

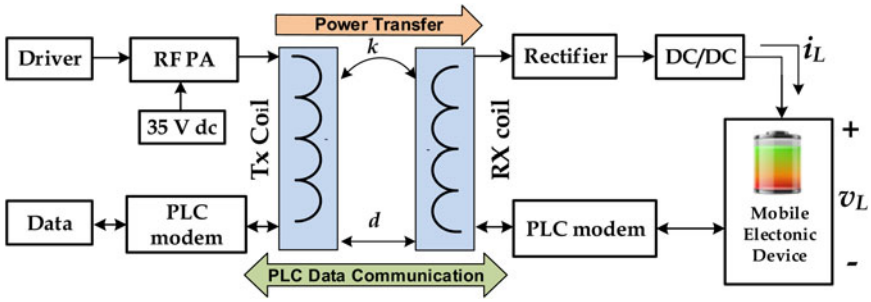

Fig. 1. Block diagram of the integrated WPT-PLC.

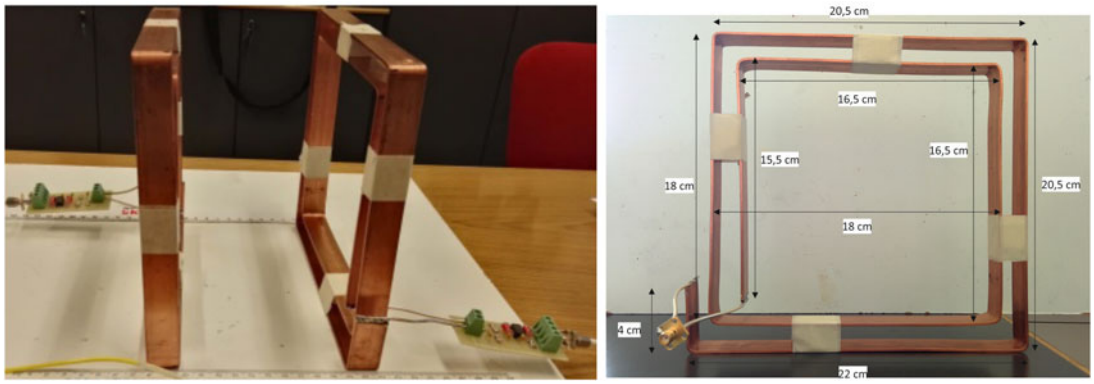

Fig. 2. Prototype coils used for characterization with coil dimensions.

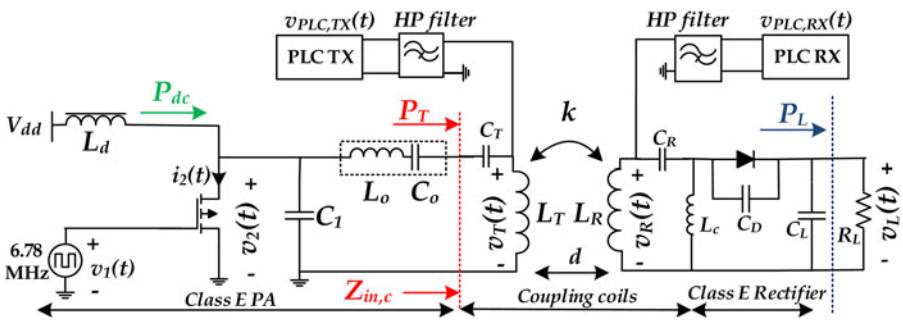

Fig. 3. Integrated WPT-PLC circuit configuration and its main electrical components and variables.

changes with the I/O loading resistance; therefore, these values were tuned in order to get the resonant channel transmission coefficient at f_0 for different separating distances. Moreover, this result is confirmed in Fig. 8 where the WPT system achieves better power efficiency at the maximum delivered power at 10 Ω.

In [23], it is shown that a power efficient GaN class-E PA can be realized using an impedance transformation network that adapts the impedance seen from the output of the GaN transistor, to match the ideal impedance of the WPT. The overall circuit used for optimizing the IMN is depicted in Fig. 4: as shown in the Smith chart of Fig. 7, the resulting Pi-shaped matching network accurately adapts the impedance at the three frequencies ω_0, $2\omega_0$, and $3\omega_0$. The optimized Pi-IMN components are $L_m = 368$ nH, $C_{m1} = 741$ pF, and $C_{m2} = 365$ pF.

Power efficient design

The designed wireless power link achieves a maximum efficiency of 90% under an optimum operating condition. However, the performance is sensitive to the variations of k and R_L. To quantify the effect of the load variation, the output power and the efficiency of the overall system (coupling coils, class-E PA and rectifier) was calculated for several load values R_L, as shown in Fig. 8. The power efficiency reaches the highest value of 94.4% when $R_L \in [14\ \Omega, 21\ \Omega]$. As R_L increases the transmitted output power P_T decreases exponentially to 8 W for $R_L = 100\ \Omega$, whereas the power efficiency performance is kept over 85% even for higher values of R_L.

In addition, the power efficiency is plotted versus different separating distances of the transmitting and receiving coils, d, as shown in Fig. 9. These results show that the deterioration of the system performance is mostly due to the load's mismatch of the wireless power link.

WPT systems working in real-world applications should be characterized also by robustness to variations. For this reason, reduced changes of the high-power output of WPT link should be guaranteed even under the variation of the load or separating distance. The output power variation could be reduced with a controllable dc power supply, but this solution may be harmful for the GaN transistor if V_{DS} values exceed $V_{DS,max}$ (shown in Table 1). Therefore, a further optimization of the IMN is required to achieve an efficient and robust high-power performance of the power link.

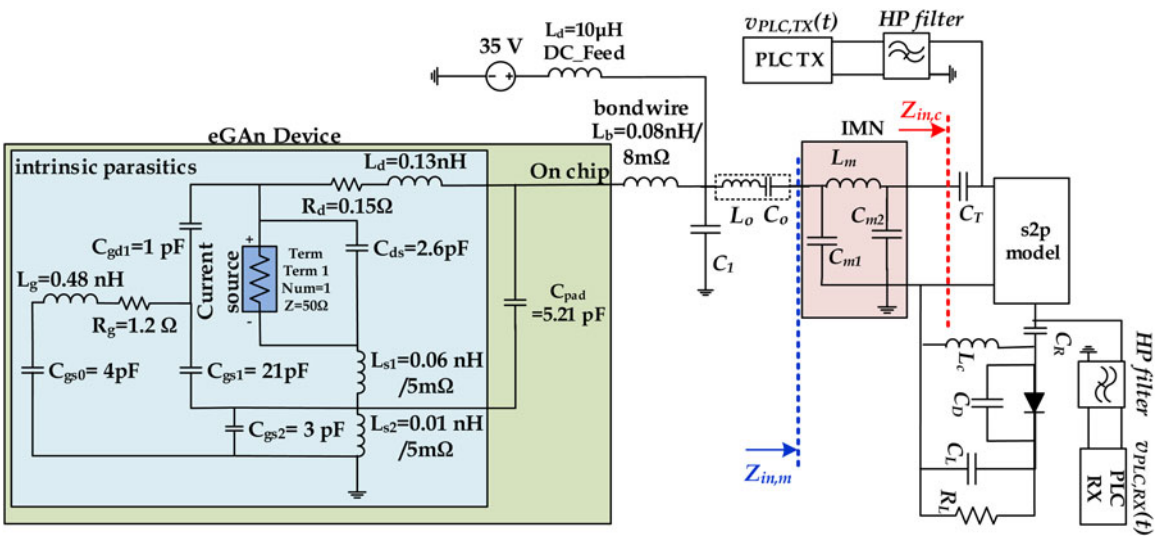

Fig. 4. Simulation setup used for optimizing the value of the matching network for matching the fundamental, second, and third harmonics.

Table 1. Typical specification of the selected eGaN FET

Parameter	Value	Parameter	Value
$V_{DS,max}$	100 V	Q_{RR}	0 nC
V_{GS}	[−4 V, 6 V]	Q_{GD}	0.6 nC
$R_{DS(ON),max}$	30 mΩ	Q_{OSS}	12.6 nC
Q_G	2.2 nC	$I_{D,DC}$	6 A
Q_{GS}	0.6 nC	$I_{D;pulsed}$	40 A

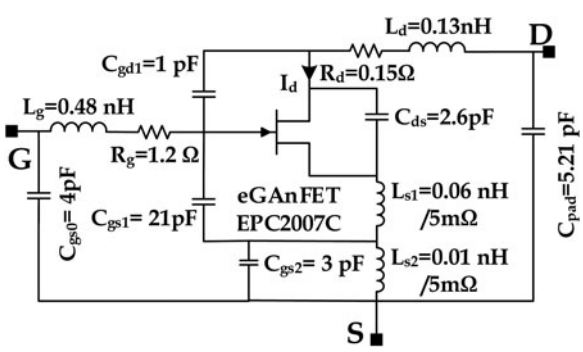

Fig. 5. Extrinsic and intrinsic parasitic components of the eGAnFET EPC2007C transistor.

L-, Pi-, and T-type are the common topologies which can be used as IMN to accomplish the most extreme power efficiency in the output [34]. In fact, the Pi- and T-type networks enable not only a higher design flexibility for impedance optimization and matching for wider range of PA's load variation but also for harmonic rejection. Despite its performance in keeping the power at a higher level, the L-type IMN will not be the proper choice in our case due to the circuit complexity and large number of lumped components; for this reason the decision (previously shown) to adopt the Pi-type IMN is confirmed also from the power performance point of view as seen in Fig. 4.

The aim of the IMN is to transform the output impedance $Z_{in,c}$ to the high efficiency region in the Smith chart and to make it close enough to the optimized impedance Z_{opt} of the class-E PA. The load pull simulation setup is used to optimize the value of C_1 and the IMN components values (C_{m1}, C_{m2}, and L_m), by means of a genetic algorithm based multi-objective optimization. The goal is to transform $Z_{in,c}(\omega_0)$ into a high efficiency region (90% efficiency contour) and, at the same time, minimizing $Z_{in,m}$ at the second and third harmonics. These conflicting objectives on the power efficiency and low harmonic distortions are formulated as follows [23–25 27]:

$$\min\left(\sum_{R_L}\sum_{d}|Z_{opt}(\omega_0)-Z_{in,m}(\omega_0)|\right) \tag{2}$$

$$\min\left(\sum_{R_L}\sum_{d}|Z_{in,m}(2\omega_0)|\right) \tag{3}$$

$$\min\left(\sum_{R_L}\sum_{d}|Z_{in,m}(3\omega_0)|\right) \tag{4}$$

The WPT-PLC system can achieve a maximum efficiency of 98% as it can be seen by the Z_{opt} point in Fig. 10, showing the results of the optimization procedure. The chart shows constant power and constant efficiency contours, calculated using the load-pull simulations relative to a variable distance d (10–30 cm) and variable R_L (10–100 Ω). The output power and the WPT-PLC efficiency decrease as the PA load deviates from the optimal value. Nevertheless, the system performance may decrease in terms of delivered power (e.g. blue contours) and high efficiency (e.g. red contours) due to the variation of the load R_L and separating distance, d. The resulting contours shown in Fig. 10 explain that the designed class-E WPT-PLC system is sensitive to load variation. Moreover, the designed IMN may ensure only a high efficiency of the WPT-PLC system but with significant varying output power as seen from the overlapping contours in Fig. 10 and the analysis of Fig. 8. For these reasons, the designed IMN can induce a large variation of the output power which is inadequate for most application. This issue can be addressed by

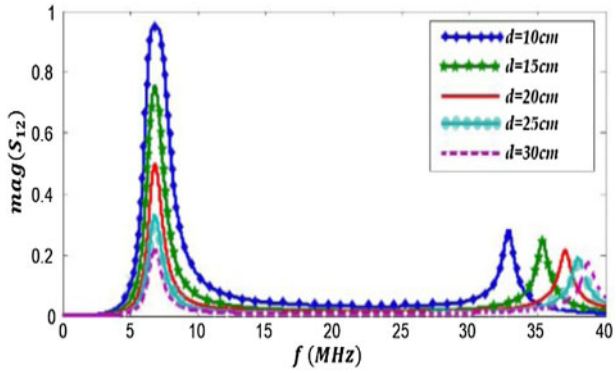

Fig. 6. VNA measured transmission coefficient magnitude of the resonant inductive channel at different separating distances.

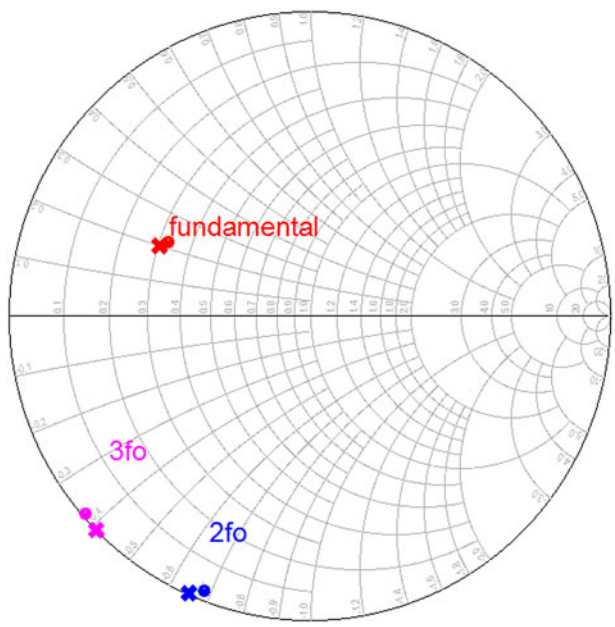

Fig. 7. Impedance matching at 6.78 MHz (fundamental f_0), at $2f_0$ and $3f_0$ ($Z_{in,c}$ (×) and the optimized Pi-IMN $Z_{in,m}$ (○)).

confining the output power by using a controlled dc power which may damage the drain voltage of the transistor.

Consequently, the designed Pi-IMN is capable of transforming all the $Z_{in,c}$ into a high-power efficient region and stable output power for a wide range of operation conditions. Moreover, the variation of $Z_{in,m}$ corresponding to the variation of d and R_L are shown by the green region S_{IMN} located within the constant efficiency contour of 92% and the optimum load of the PA, Z_{opt}. At the same time, the output power is stable and varies between 34.54 and 38.17 W. Table 2 shows the parameter values after optimization.

PLC and WPT integration validation

Figure 11 shows the model used for the validation of the designed system, with the aim of verifying whether the design procedure defined here complies with the objective of the work, i.e. high efficiency power transfer and low harmonics to improve PLC data transfer.

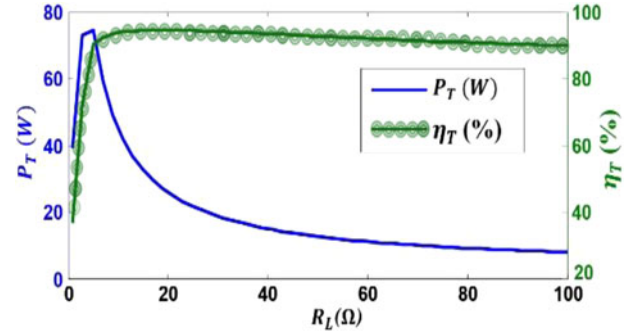

Fig. 8. Output power (P_T), and power efficiency (η_T) versus R_L (with $d = 10$ cm).

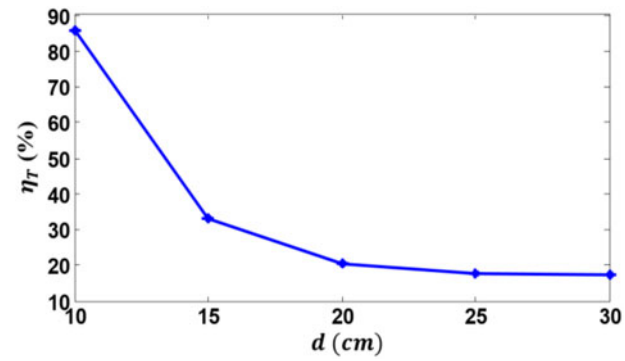

Fig. 9. Power efficiency η_T as a function of d (with $R_L = 50\ \Omega$).

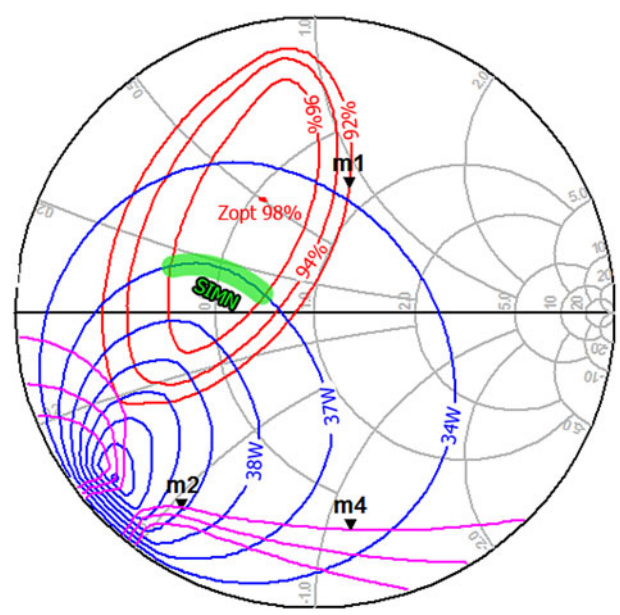

Fig. 10. Load-pull simulation results of the optimized WPT-PLC system and $Z_{in,m}$ with varying d (10–30 cm) and R_L (10–100 Ω). Constant power contour (blue dashed line), constant power efficiency contour (red solid line), equivalent PA load variation S_{IMN} (green region).

Power link validation

Figure 12 illustrates the transient waveforms of the transistor output voltage $v_2(t)$, and current $i_2(t)$, showing the realistic zero voltage and current switching due to the parasitic dynamics.

Table 2. Circuit optimized parameters values of the WPT-PLC system

Parameter	Value	Parameter	Value
C_{m1}	760 pF	C_L	40 µF
C_{m2}	580 pF	V_{DC}	35 V
L_m	420 nH	$v_{1,low}$	0 V
$C_R = C_T$	712 pF	$v_{1,peak}$	−4 V
C_D	145 pF	V_{1DC}	0 V
L_c	20 µF	C_1	214 pF

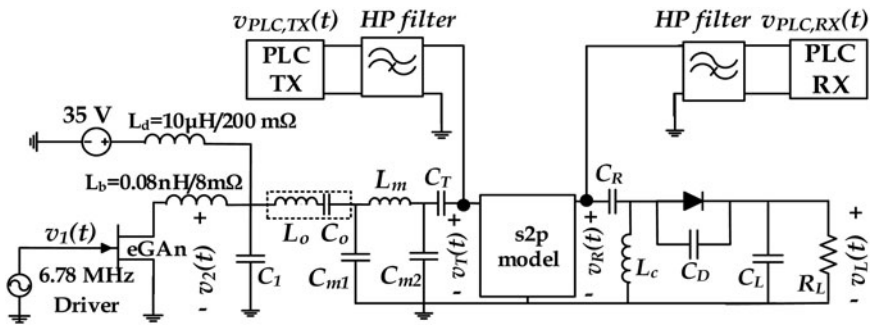

Fig. 11. Validation setup of the integrated WPT-PLC system.

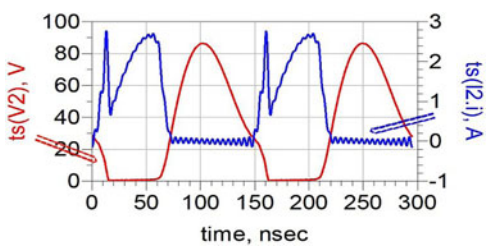

Fig. 12. Source current and drain voltage waveforms of the eGaN FET-based class-E PA.

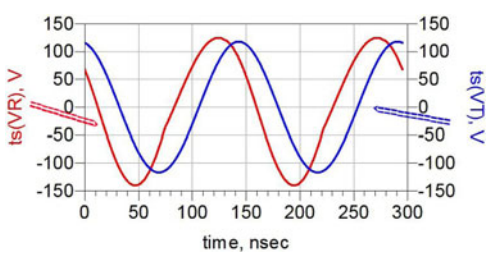

Fig. 13. Time domain waveforms at the WPT transmitting and receiving coils.

This real-modeling scenario captures the conduction and the switching losses which contribute to the increase of the dissipated power (i.e. reducing the power efficiency). The predicted output voltages at the transmitting and receiving coils of the previous simulated setup are shown in Fig. 13.

The class-E PA, which is driven into saturation by the switching PWM input signal, generates a distorted sinusoidal power signal. The spectrums of the time domain voltage waveforms illustrating the harmonic distortions at the transmitting and receiving coils are shown in Fig. 14. Since the wireless inductive channel is selective in frequency and has a band-pass

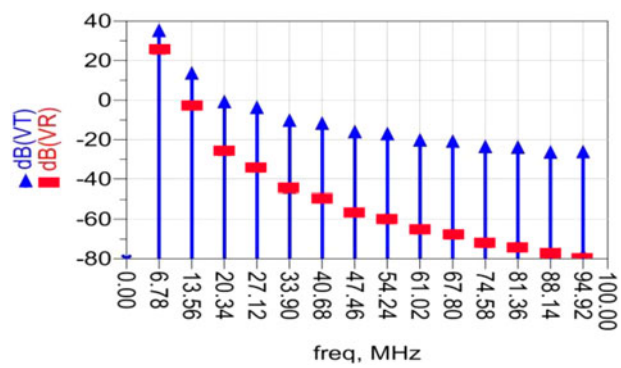

Fig. 14. Spectrum of voltages at the transmitting and receiving coils.

characteristic, the harmonic frequencies of the transmitted output voltage are differently attenuated.

One way to reduce the magnitude of the harmonic distortions is to use sine-driven class-E PA: the power efficiency over a 10 cm separating distance, along with the total harmonic distortion (THD) for the pulse and sine-driven class-E PA, are reported in Table 3, in which THD of a signal $x(t)$ is defined in (5) where x_n stands for the n-th harmonic:

$$THD_x\ (\%) = \frac{100\left(\sqrt{\sum_n^{\infty} x_n^2}\right)}{x_1} \tag{5}$$

When using a sine-driven class-E wireless power link, a THD reduction ratio of 47.36%, is achieved at the transmitting coil (THD_{v_T}) and of 80.43% at the receiving coil (THD_{v_R}). However, the total dissipated power of the WPT-PLC system is increased by 2.7 W due to the rise of the conducting losses between the transistor states caused by the ON/OFF switching, which is not as short as the pulse-driven class-E PA. Consequently, the transmitted power

Table 3. Simulation results of the optimized WPT-PLC system

Pulse-driven class-E PA				Sine-driven Class-E PA			
P_{dc}	32.6 W	THD_{v_2}	36.3%	P_{dc}	35.3 W	THD_{v_2}	27.2%
P_L	27.1 W	THD_{v_T}	11.4%	P_L	27.1 W	THD_{v_T}	6.0%
P_{dis}	5.5 W	THD_{v_R}	2.3%	P_{dis}	8.2 W	THD_{v_R}	0.45%
η_T	90.4%	η_{ee}	83.2%	η_T	86.5%	η_{ee}	76.7%

efficiency η_T, and the end to end power efficiency η_{ee}, are reduced by 7.69 and 11.32%, respectively. A dc–dc regulator can be used after the rectifier circuit in order to adopt the proposed WPT-PLC design technique for various applications and loading conditions.

Noise and interference mitigation

From a regulatory point of view, the IEC CISPR has classified WPT applications into three classes according to their capability to allow data communication at a particular frequency band [27]. The PLC signal of the proposed WPT-PLC application uses different frequency ranges than those used for WPT. Therefore, the proposed integrated WPT-PLC system can be classified, according to [27], in class C. Recently, a new revision to ETSI test standard EN 300 330-2 has added WPT for devices that include data communication function [35]. Accordingly, the conducted voltage disturbance limit at the mains terminals on class-A WPT transmitters and receivers ports (in the frequency range of 0.5–30 MHz) is 73 dB (μV), which corresponds to −34 dBm [24, 25]. As seen in Fig. 15(a), the power of the generated frequencies at the PLC transmitter ($v_{PLC,TX}$) and receiver ($v_{PLC,RX}$) ports become smaller than the specified threshold of −34 dBm only as the frequency exceeds the third harmonic (e.g. 20.34 MHz). Moreover, the harmonic distortions are increased due to the nonlinear dynamic of the rectifying diode, and the conducted EMC limit was violated in the considered scenario as shown in Fig. 15(b).

Since the harmonic distortions induced by the class-E PA and rectifier are deterministic and their positions can be determined a priori, advanced interference rejection/blocking HP filters and high Q circuitry can be used to attenuate the harmonics [23, 28]. PLC technology offers reliable and high data rate communication by means of multi-carrier orthogonal frequency division multiplexing modulation (OFDM) schemes in a noisy environment. Indeed, the broadband (BB) PLC physical layer uses OFDM carriers spaced at 24.414 kHz, with carriers from 2 to 30 MHz. Also, the IEEE 1901 standard extends this range optionally to 50 MHz and many BB-PLC specifications, such as the HomePlugAV2, extends the frequencies in the range of 30–86 MHz which will enable higher data rates of hundreds of Mbps aside from WPT interferences.

The designed WPT system operates at 6.78 MHz which is in a close proximity with the BB-PLC band, this raises EMC issues due to the power levels of the harmonic distortions generated by means of the class-E PA and rectifier's nonlinearity, that acts as a narrowband interference with respect to PLC. In particular, narrowband interference was shown to be detrimental for OFDM symbol demodulation [36]. The use of a cancelation/mitigation techniques [37, 38] is then required, and in general these methods are able to significantly reduce the effect of the narrowband interference, allowing acceptable bit error rates even under unfavorable conditions up to 30 dB of signal attenuation [36].

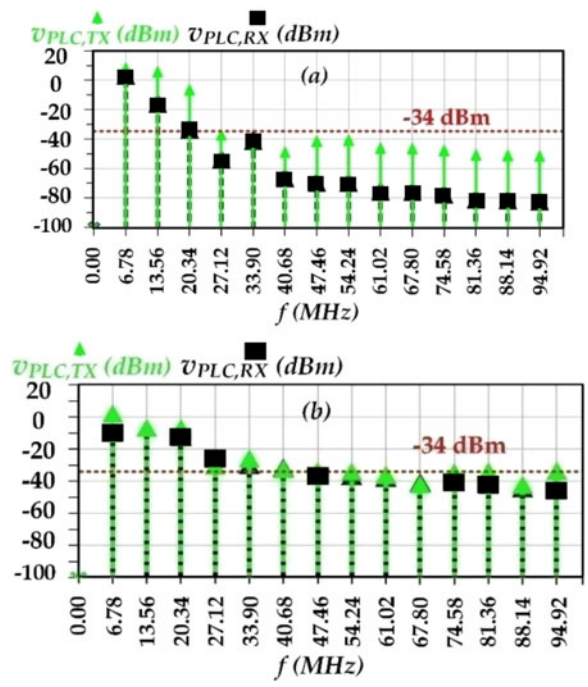

Fig. 15. Spectrum of voltages at the PLC transmitter and receiver's ports relative to a sine-driven PA of the WPT link: (a) without a rectifier and (b) with a rectifier.

Channel capacity

The effects of harmonic distortions introduced by the wireless power link on the capacity C of the communication channel can be estimated by the Shannon–Hartley's formula that reads as

$$\begin{cases} C = B\log_2\left(1 + \dfrac{S(f)}{I(f) + N(f)}\right) \\ S(f) = S_t(f)|H(f,d)|^2 \end{cases} \tag{6}$$

where$S(f)$ is the power spectral density of the received communication signal, $N(f)$ is the random noise spectral density at the receiver, and $I(f)$ is the narrowband interference power produced by the WPT circuit. B is the channel bandwidth, $S_t(f)$ is the transmitted signal's spectral density, and $H(f, d)$ is the communication channel's transfer function. In previous studies [11–15], the channel capacity was calculated using equation (6) in the case of $I(f) = 0$, $N(f) = N_0/2$ corresponding to AWGN, and constant transmitted power $S_t(f) = S_t/2$ in the frequency range from 7 up to 30 MHz. It was shown that for a distance $d = 10$ cm, the capacity ranges from 33.5 kbit/s to 4.4 Mbit/s, when a signal to noise ratio, S_t/N_0, ranges between −2 and 20 dB.

In order to evaluate the effect of the interference $I(f)$, which is shown in Fig. 14(b), we consider a sinc-shaped PSD around each harmonic, with a main lobe bandwidth of 48.8 kHz (twice the distance between carriers in HomePlug AV).

Three harmonics are involved, for instance 13.56, 20.34, and 27.12 MHz. As a result, we obtain that the channel capacity C is reduced by about 5% compared to the case $I(f) = 0$. This result indicates a moderate effect of the harmonic distortions introduced by the designed PA on the PLC communication.

Conclusion

This paper presents the design considerations required to guarantee an optimal performance of the integrated WPT-PLC system in the presence of harmonic interferences. The analysis of the non-linear harmonic distortions generated by the proposed sine-driven class-E wireless power link and their effects on the channel capacity of the broad band PLC link, are investigated and evaluated to ensure a reliable WPT-PLC system. These findings are achieved by designing the IMN to meet the constraints of high-power efficiency and low THD based on the *S*-parameters and load pull simulation results. Moreover, mitigation solutions that the PLC transceivers already offer to avoid the deterministic harmonics interference were discussed. Therefore, careful high-power WPT system design considerations must be taken to ensure reliable PLC data communication through the resonant inductive channel.

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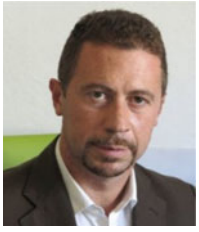

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